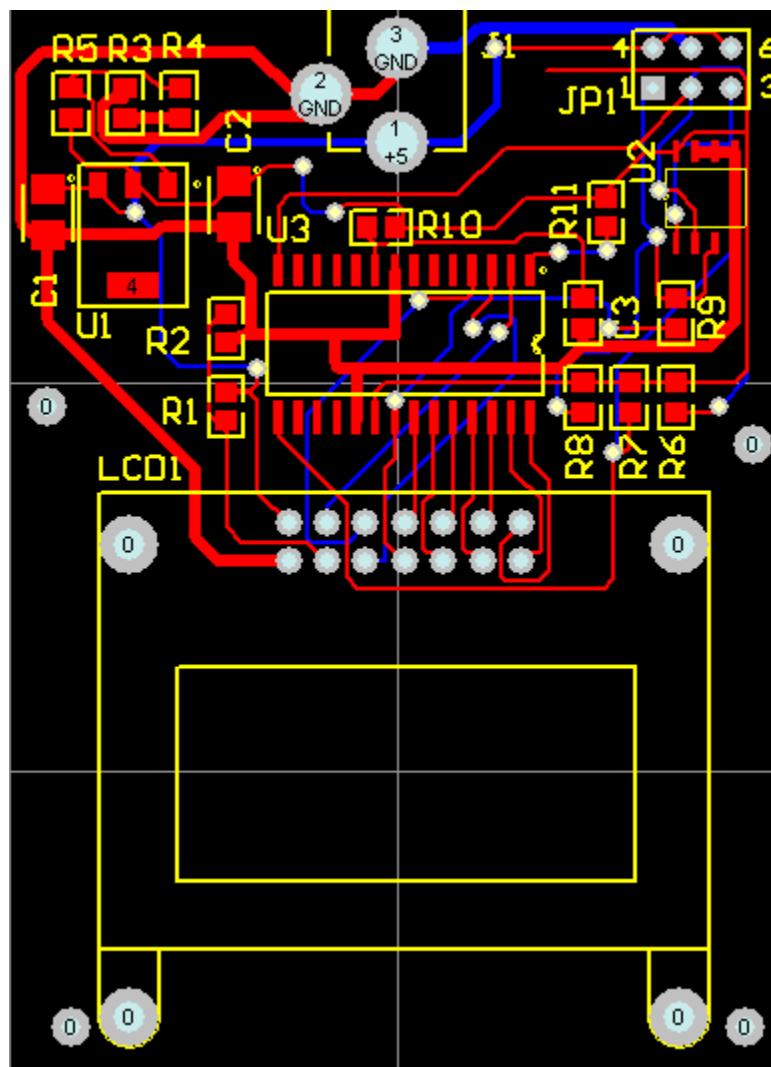


Prepare by : HK Sim simhkeng@gmail.com

Date : 22 Dec 05



Prepare by : HK Sim simhkeng@gmail.com

Main steps from Schematic to PCB

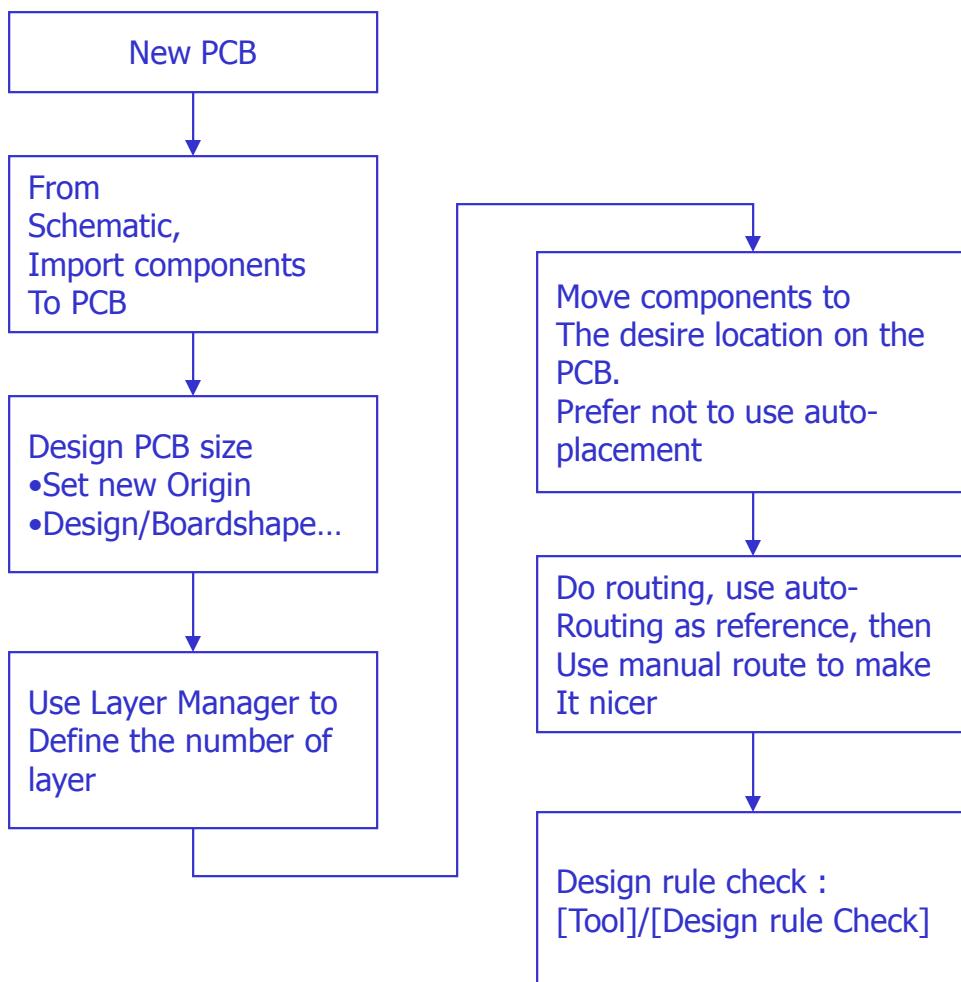
Move from schematic to PCB

Define PCB size

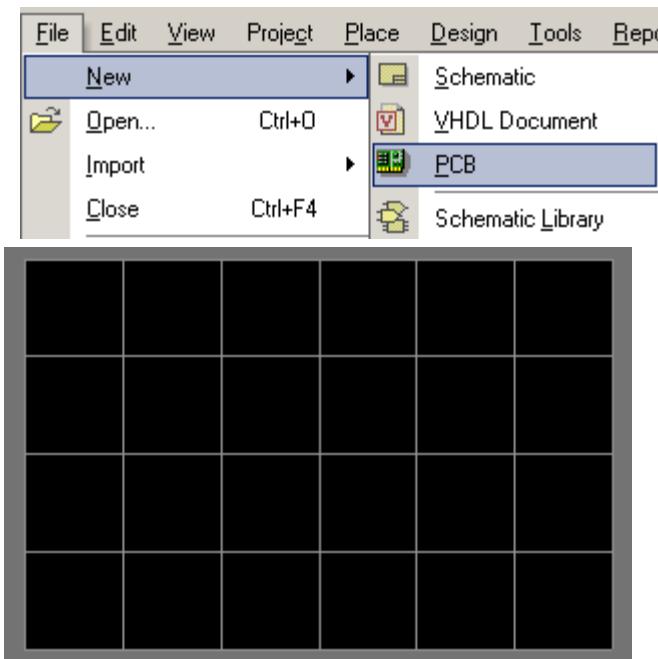
Bring component from schematic to PCB

Move the components to the desire position

Layout the path



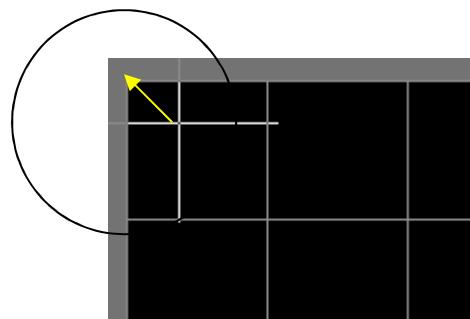
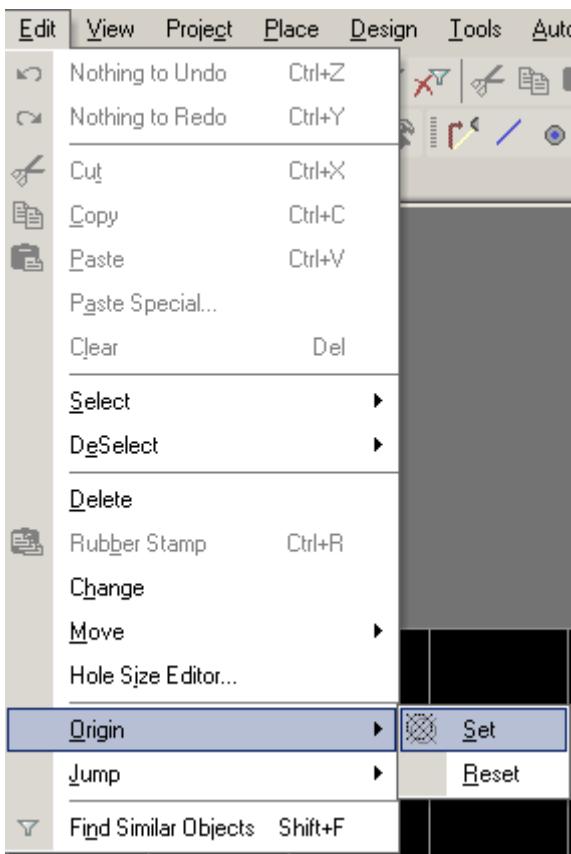
Move from schematic to PCB



Define PCB size

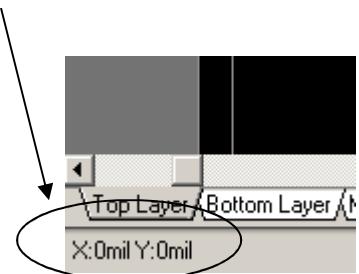
[Set reference Origin on PCB](#)

[\[Edit\] / \[Origin\] / \[Set\]](#)



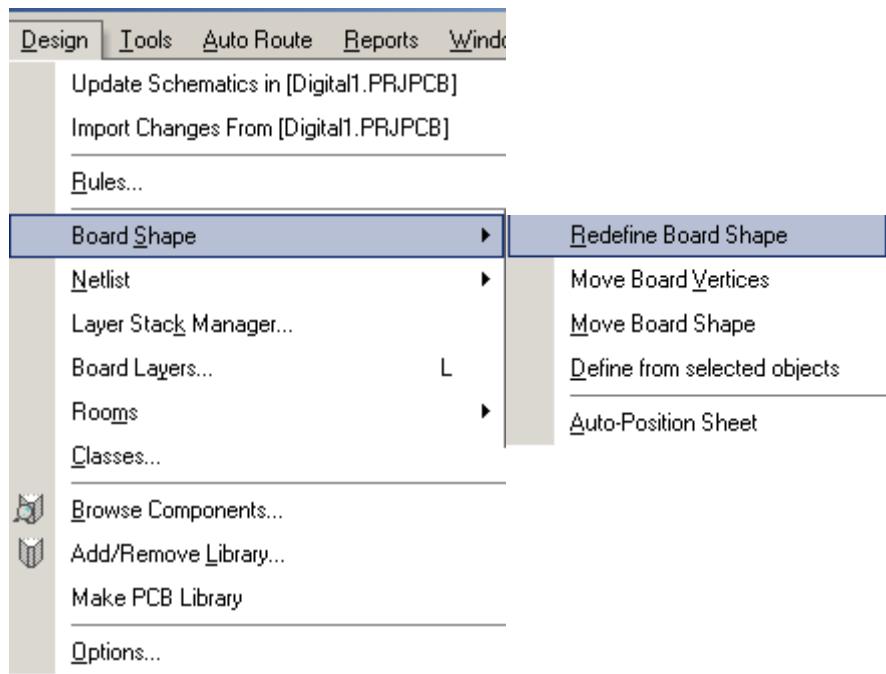
Move the cursor to the point that you want to set as origin and click.

After that, this point's position should read as [0,0]

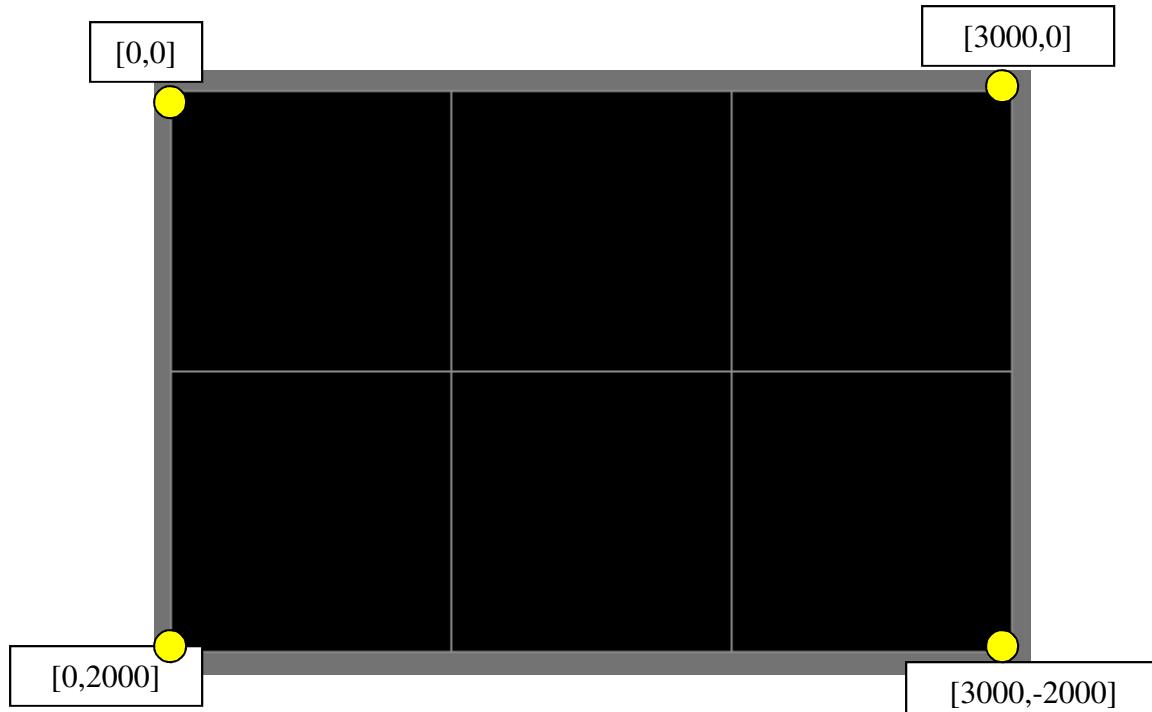


Change the board shape use

[Design]/[Board Shape]/[Redefine Board Shape]

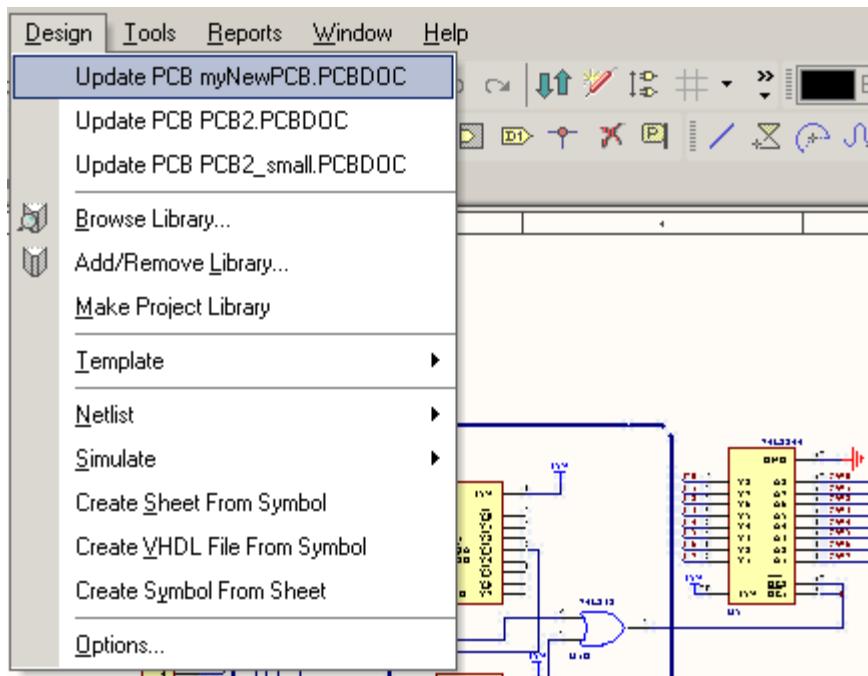


The PCB will change from black to green. Start from the set origin [0,0], use the mouse to move around in a close rectangle box to define the board side. See the bottom co-ordinate to know the dimension.



Bring component from schematic to PCB

To bring components from schematic into PCB , while you are in the schematic ,use the following to bring the component to the correct PCB



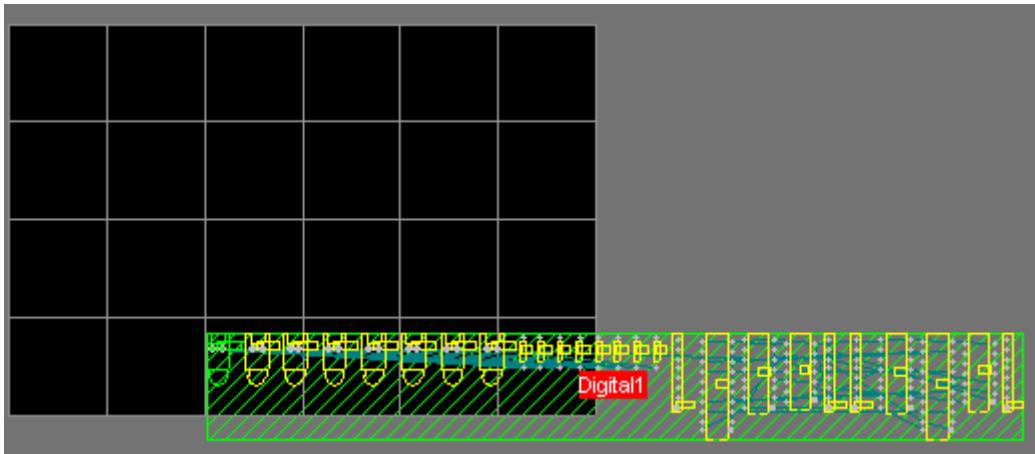
This because when the PCB have no components, update the specified PCB will bring all components from the schematic into the PCB.

Modifications			
Action	Affected Object	To	Affected Document
Add Components(26)			
Add	JP1	To	Digital1.PCBDOC
Add	JP2	To	Digital1.PCBDOC
Add	JP3	To	Digital1.PCBDOC
Add	JP4	To	Digital1.PCBDOC
Add	LED0	To	Digital1.PCBDOC
Add	LED1	To	Digital1.PCBDOC
Add	LED2	To	Digital1.PCBDOC
Add Nets(28)			
Add	+5V	To	Digital1.PCBDOC
Add	AEN	To	Digital1.PCBDOC
Add	D0	To	Digital1.PCBDOC
Add	D1	To	Digital1.PCBDOC
Add	VCC	To	Digital1.PCBDOC
Add Component Classes(1)			
Add	Digital1	To	Digital1.PCBDOC
Add Rooms(1)			
Add	Room Digital1 (Scope=InComponentC	To	Digital1.PCBDOC
<input type="button" value="Validate Changes"/>		<input type="button" value="Execute Changes"/>	<input type="button" value="Report Changes..."/>

Click [Validate Changes] to check if there is any error .

Click [Execute Changes] to initiate the change.

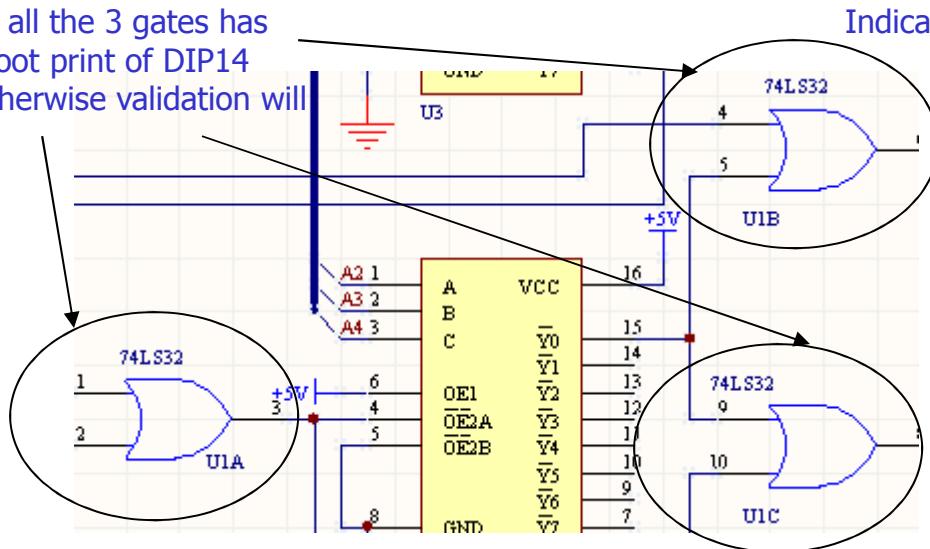
After click Execute Changes, component footprints are brought into PCB



Error example.

Add	R8	To	Digital1.PCBDOC	✓
Add	U1	To	Digital1.PCBDOC	✗
Add	U2	To	Digital1.PCBDOC	✓
Add	U3	To	Digital1.PCBDOC	✗
Add	U4	To	Digital1.PCBDOC	✗
Add	U5	To	Digital1.PCBDOC	✓
Add	U6	To	Digital1.PCBDOC	✗

Make sure all the 3 gates has common foot print of DIP14 picture, otherwise validation will give error.



Indicate there is error

Update changes between Schematic and PCB

During the layout of PCB, when make changes on schematic, can use the following method to update the PCB :

[Project] / [compile PCB project] – if there is no logical error, the compilation will be quiet . I.e Nothing display

Use update PCB as follows :

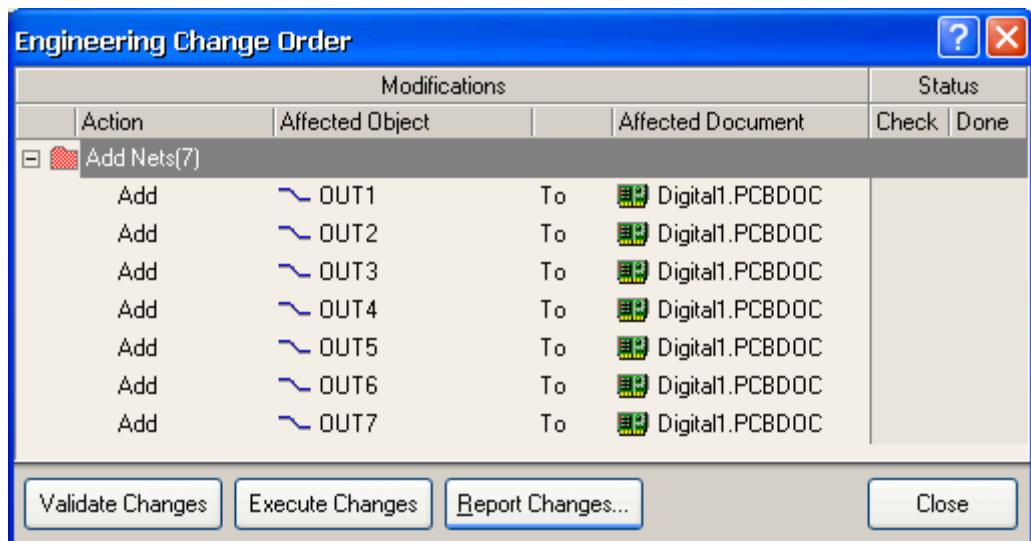


A list of different items (different from the previous PCB) is then displayed.

Use [Validate Changes] – to check the changes

Use [Execute Changes] – to implement the changes. Then the PCB will be updated with the new changes

Use [Close] – to end changes

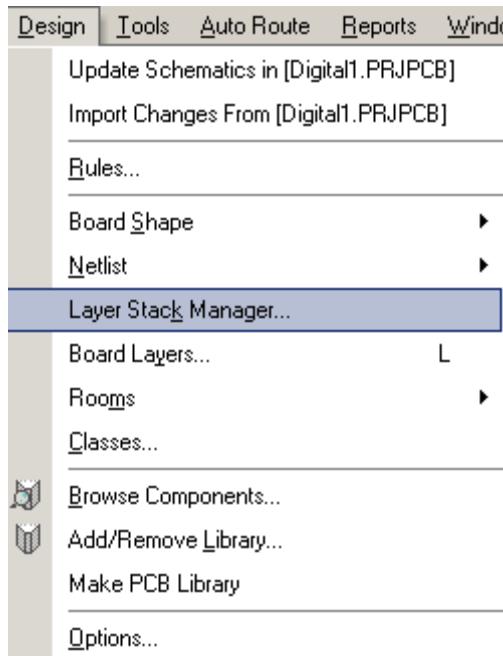


Modifications				Status	
Action	Affected Object		Affected Document	Check	Done
Add	OUT1	To	Digital1.PCBDOC		
Add	OUT2	To	Digital1.PCBDOC		
Add	OUT3	To	Digital1.PCBDOC		
Add	OUT4	To	Digital1.PCBDOC		
Add	OUT5	To	Digital1.PCBDOC		
Add	OUT6	To	Digital1.PCBDOC		
Add	OUT7	To	Digital1.PCBDOC		

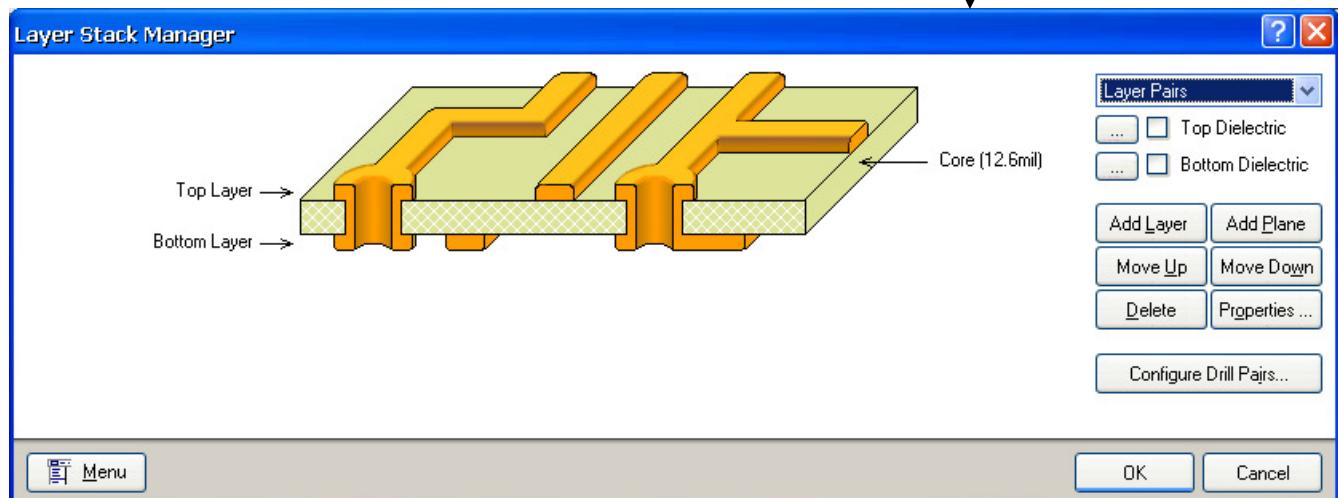
Buttons at the bottom: Validate Changes, Execute Changes, Report Changes..., Close

Add more layer to the PCB

[Design]/[Layer Stack Manager]



By default is a 2 layer PCB



Layer definition

Signal layers

Top layer
mid layer 1 to 30
Bottom layer

Internal Planes

- 16 layers available for Power/Gnd planes.
- Net can be assigned to these layers .
- Multi-layer pads and via automatically connect to these planes. Plane layers can be split into any number of regions and each regions can be assigned to different net
- Objects that are placed on the plane define regions of no copper

Silkscreen layers

Top and bottom layers for User to display component outlines

Mechanical layers

16 mechanical layers are provided for fabrication and assembly detail such as dimensions, alignment targets, annotation or other details.

Solder Mask

Top and bottom solder mask layer

Paste mask

Top and bottom paste mask layers are provided to generate the artwork which is used to manufacture stencils to deposit solder paste onto surface mount pads on PCB with surface mount devices.

Drill Drawing

Showing a unique symbol for each hole size at each location. 3 symbol styles : coded symbol, alphabetical codes (A, B, C etc) or the assigned size.

Drill Guide

Plots all holes in the layout. Drill guide is also call pad masters

Keep out area

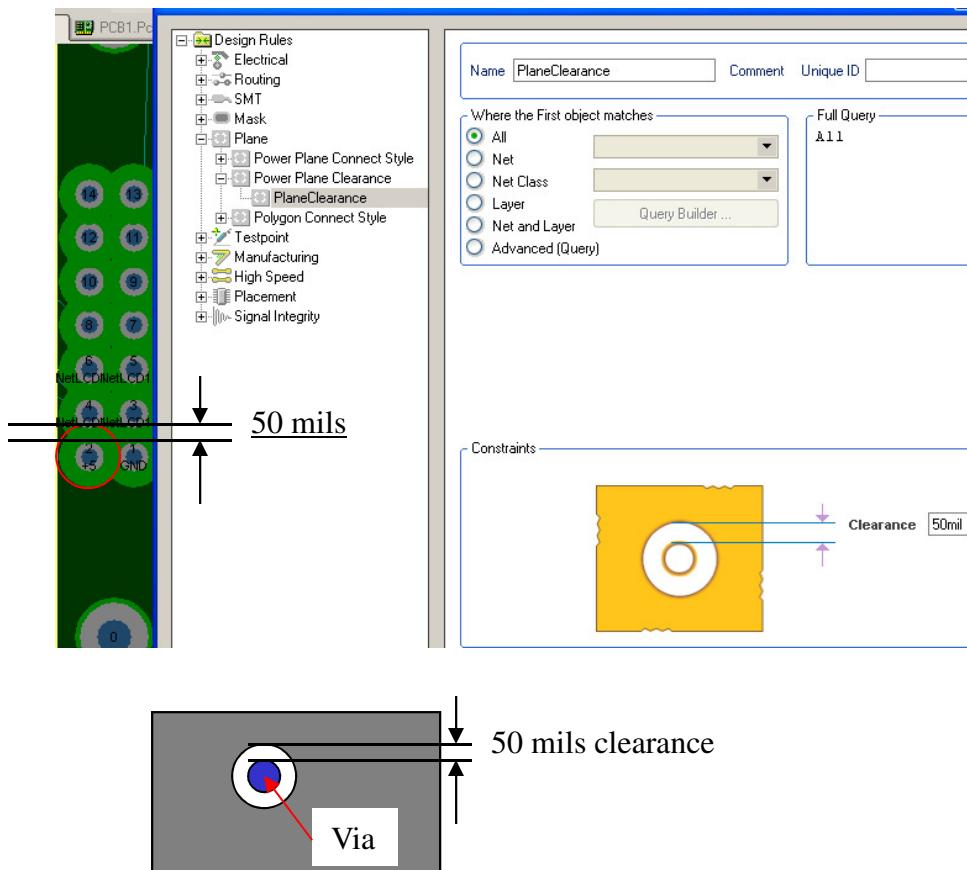
Define the regions where components and routes can validly be placed.

Components cannot be placed over an object on the keep out layer and routes cannot cross an object on the keep out layer

Multi-layer

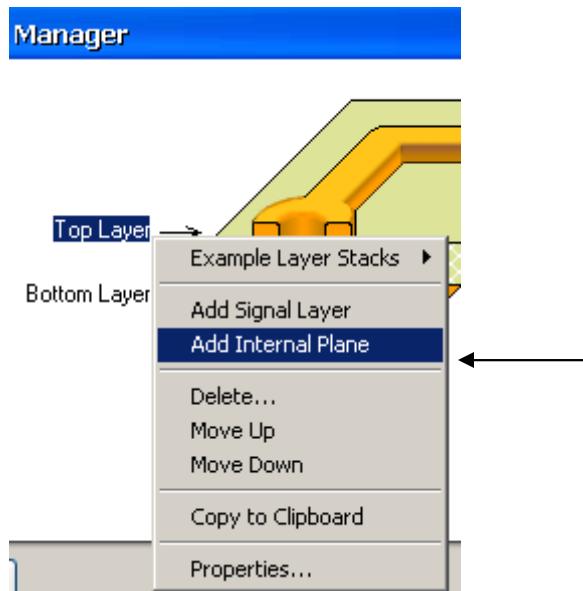
Objects placed on this layer will appear on all copper layers. This is typically use for through hole pads and via.

Power Planes Clearance setting

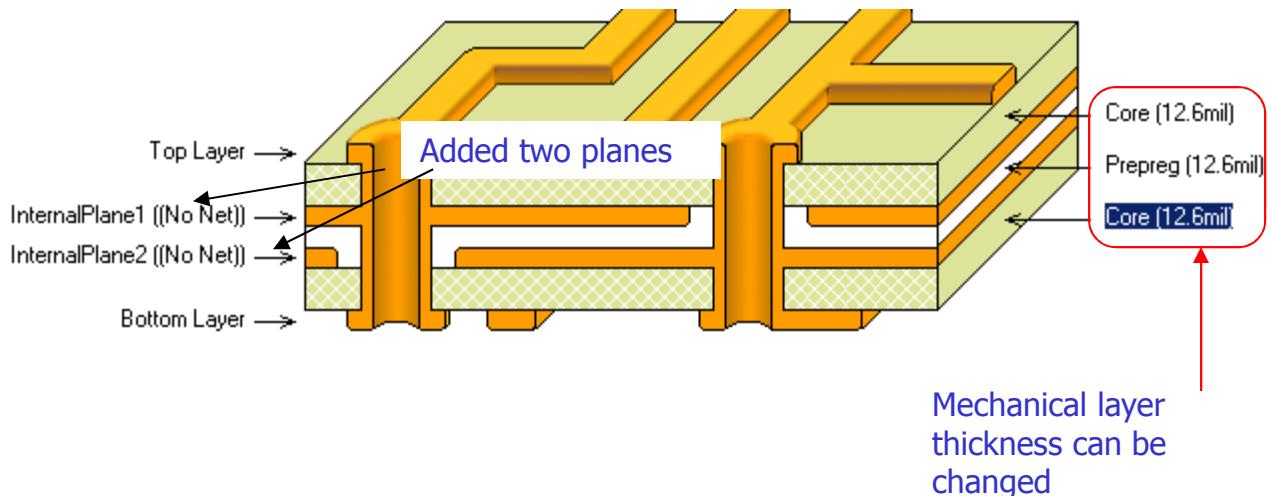


Add internal Planes

Add internal plan means Power / ground plan. It is normally 2nd plane is ground plan and 3rd plan is power plan

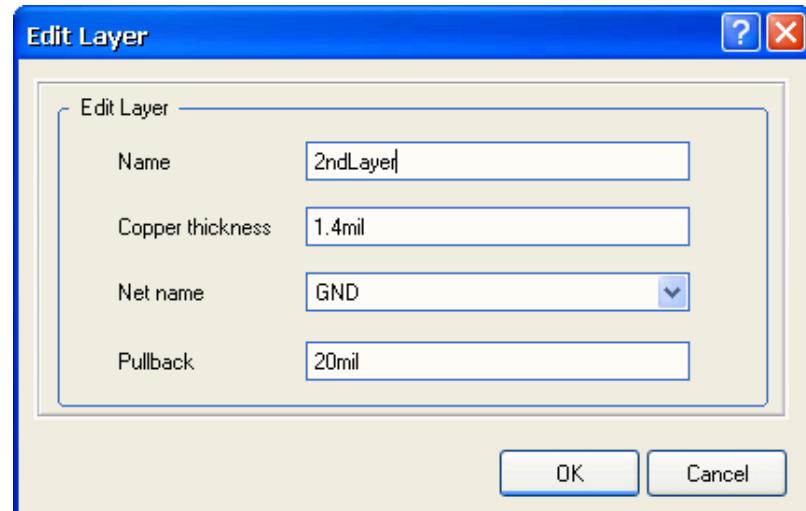


Select top layer, Right click and select Add internal plane or Signal layer



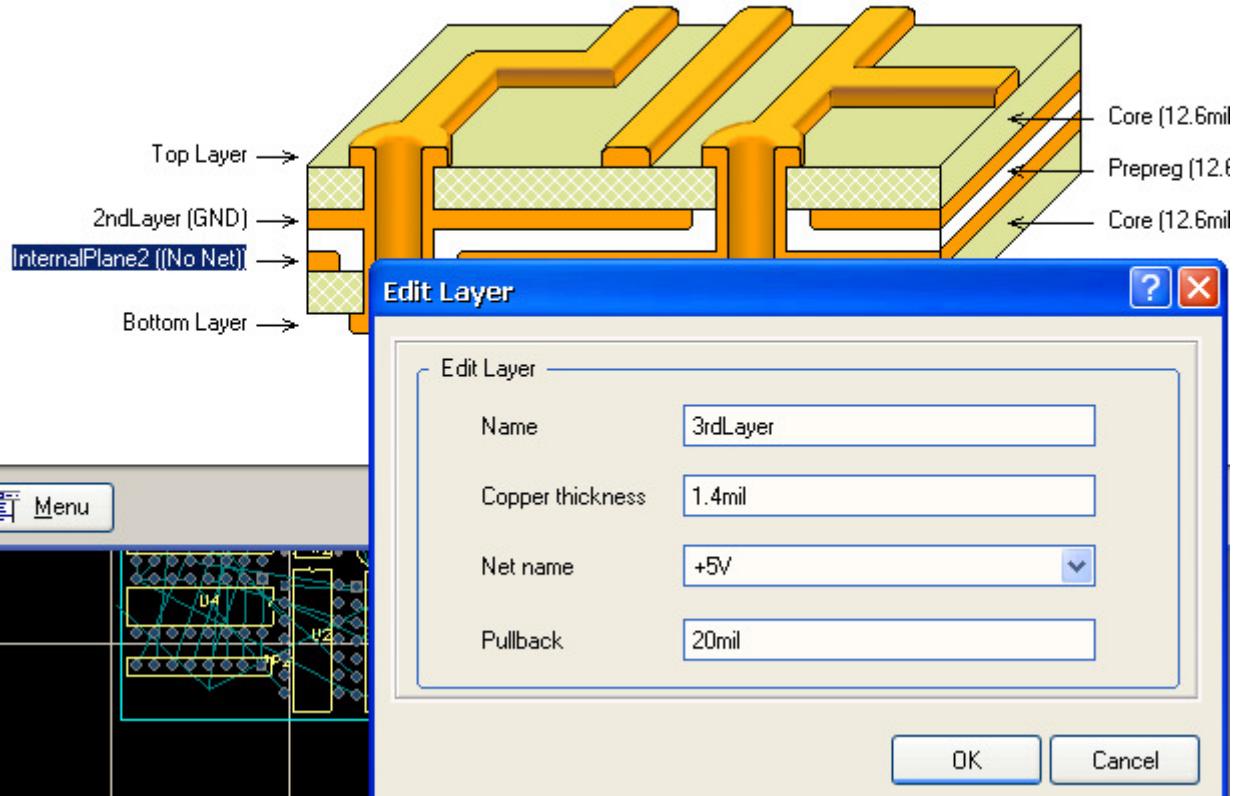
Add internal Planes

Add ground plane, Net name is GND as in schematic



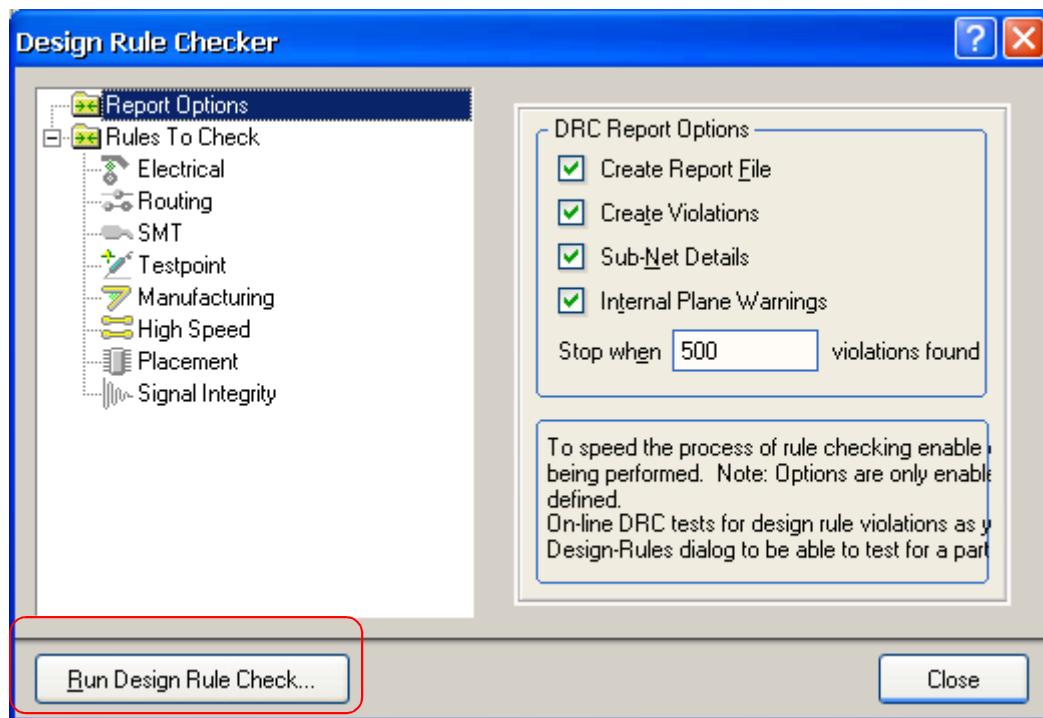
Add Power (+5V) plane, Net name is +5V as in schematic

↓
Hier Stack Manager



Design Rule Check for PCB Layout

[Tool]/[Design Rule Check]



```
Protel Design System Design Rule Check
PCB File : \simHW\Digital1\PCB2_small.PCBDOC
Date      : 12/6/2005
Time      : 7:08:14 PM

Processing Rule : Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Rule Violations :0

Processing Rule : Width Constraint (Min=10mil) (Max=10mil) (Preferred=10mil) (All)
Rule Violations :0

Processing Rule : Clearance Constraint (Gap=10mil) (All), (All)
Rule Violations :0

Processing Rule : Broken-Net Constraint ( (All) )
Rule Violations :0

Processing Rule : Short-Circuit Constraint (Allowed=Not Allowed) (All), (All)
Rule Violations :0

Violations Detected : 0
Time Elapsed       : 00:00:00
```

← Zero error !

Design Rule Setting

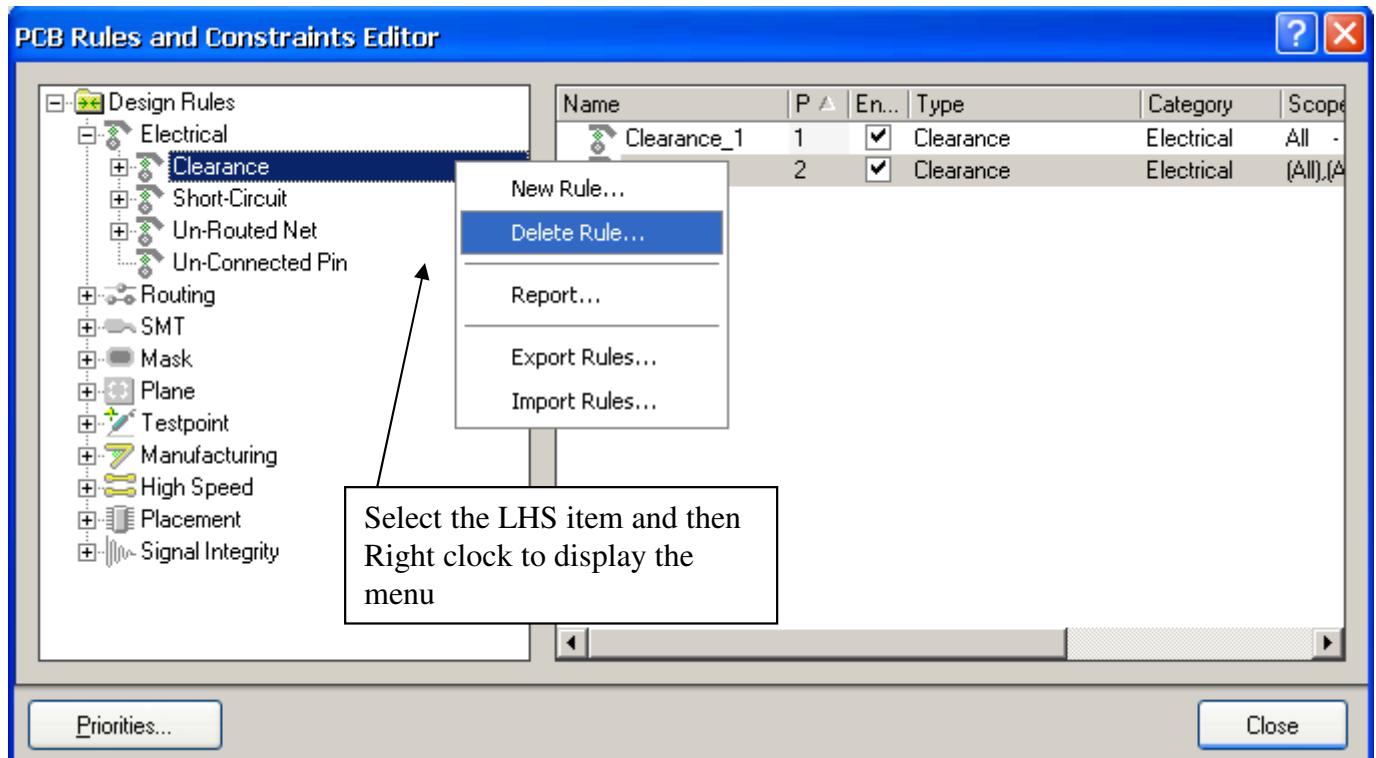
[Design] / [Rule]

PCB Rules and Constraints Editor

Name	P	En...	Type	Category	Scope	Attributes
SolderMaskExpa1		<input checked="" type="checkbox"/>	Solder Mask Expansion Mask	All		Expansion = 4mil
RoutingTopology 1		<input checked="" type="checkbox"/>	Routing Topology	Routing	All	Topology - Shortest
RoutingVias 1		<input checked="" type="checkbox"/>	Routing Via Style	Routing	All	Pref Size = 50mil
PasteMaskExpar 1		<input checked="" type="checkbox"/>	Paste Mask Expansion	Mask	All	Expansion = 0mil
TestPointUsage 1		<input checked="" type="checkbox"/>	Testpoint Usage	Testpoint	All	Testpoint - Required
LayerPairs 1		<input checked="" type="checkbox"/>	Layer Pairs	Manufacturing	All	Layer Pairs - Enforce
HoleSize 1		<input checked="" type="checkbox"/>	Hole Size	Manufacturing	All	Min = 1mil Max = 10
Testpoint 1		<input checked="" type="checkbox"/>	Testpoint Style	Testpoint	All	Under Comp - Allow
ComponentCleara1		<input checked="" type="checkbox"/>	Component Clearance	Placement	All - All	Clearance = 10mil
RoutingCorners 1		<input checked="" type="checkbox"/>	Routing Corners	Routing	All	Style - 45 Degree
Clearance 1		<input checked="" type="checkbox"/>	Clearance	Electrical	All - All	Clearance = 10mil
PlaneConnect 1		<input checked="" type="checkbox"/>	Power Plane Connect	S Plane	All	Style - Relief Connect
ShortCircuit 1		<input checked="" type="checkbox"/>	Short-Circuit	Electrical	All - All	Short Circuit - Not All
UnRoutedNet 1		<input checked="" type="checkbox"/>	Un-Routed Net	Electrical	All	(No Attributes)
PlaneClearance 1		<input checked="" type="checkbox"/>	Power Plane Clearance	Plane	All	Clearance = 20mil
RoutingPriority 1		<input checked="" type="checkbox"/>	Routing Priority	Routing	All	Priority = 0
RoutingLayers 1		<input checked="" type="checkbox"/>	Routing Layers	Routing	All	TopLayer - Horizontal
PolygonConnect 1		<input checked="" type="checkbox"/>	Polygon Connect Style	Plane	All	Style - Relief Connect
Width 1		<input checked="" type="checkbox"/>	Width	Routing	All	Pref Width = 10mil

Priorities... Right click to provide hard copy of report Close

Select item at the LHS box and do a right click, you can add / delete rules ... etc

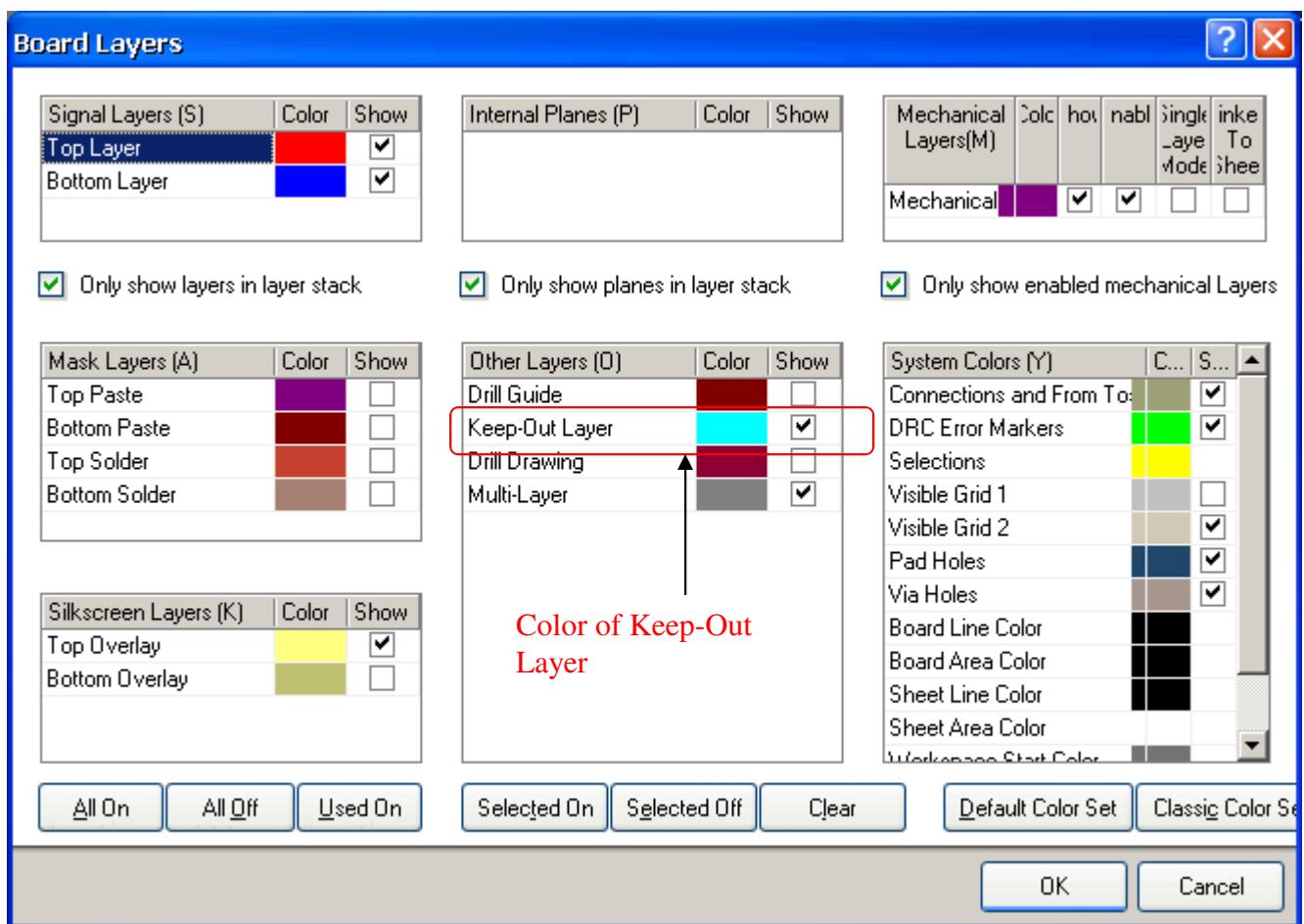


Auto Placement

It is recommended that key component should not use auto-placement due to performance and appearance.

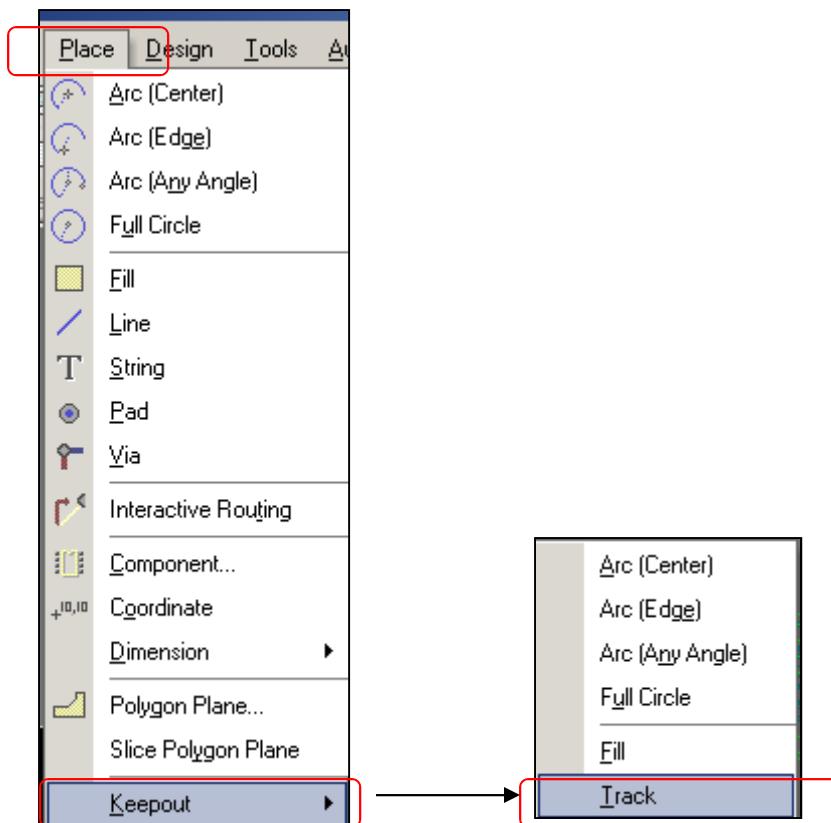
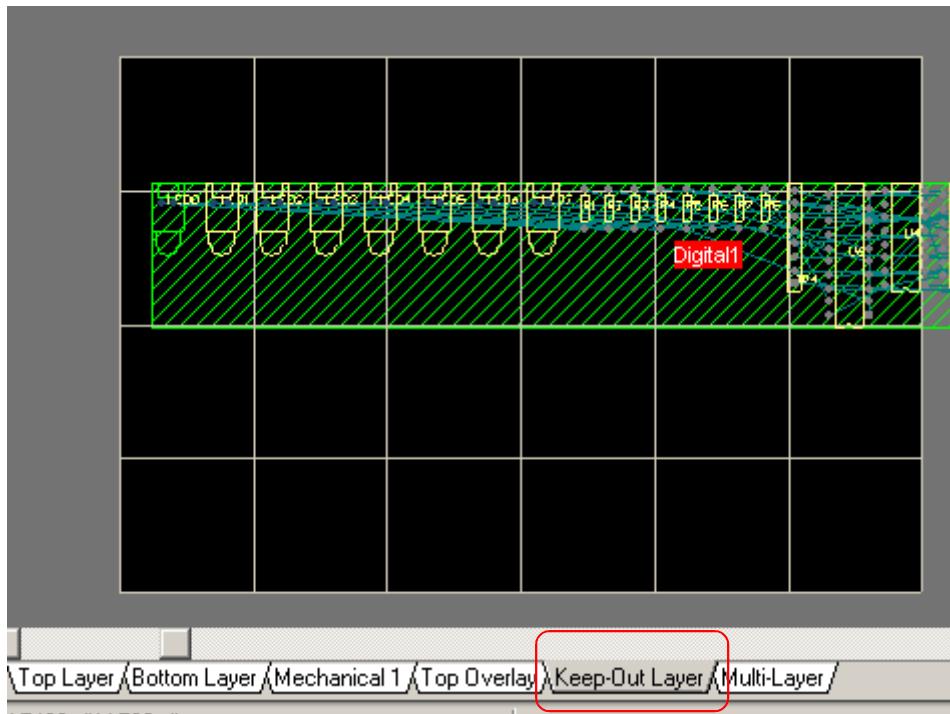
To do an auto-placement, you **must define** the keep-out area where no routing will be pass through that area..

Keep-out area can defined on the Keep-out Layer

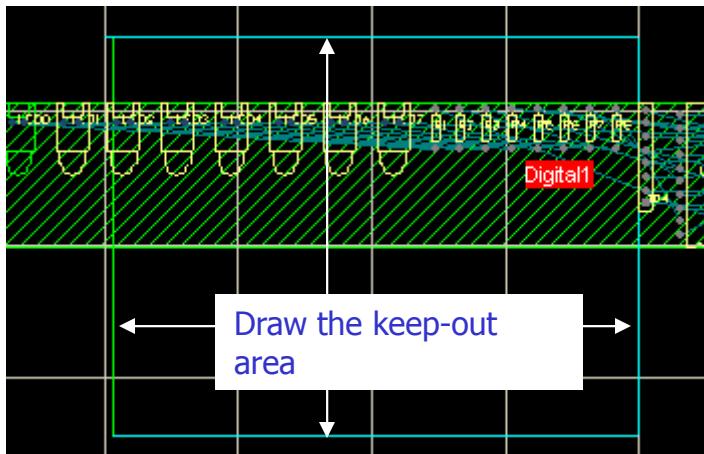


Short cut to get this menu Press **L** on the PCB board

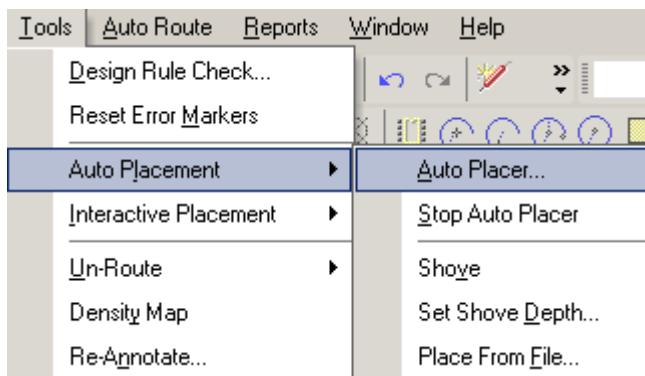
Define Keep Out Area



Draw the keep out area



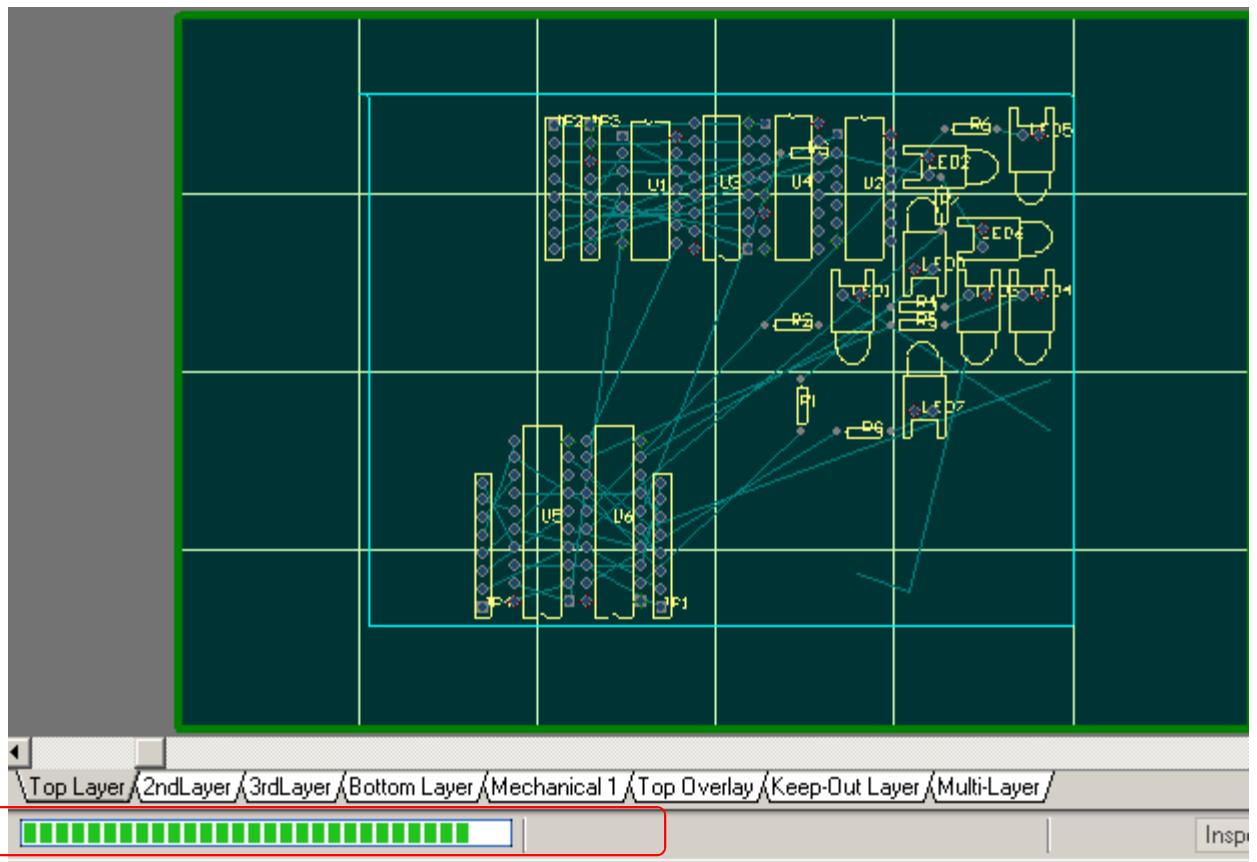
After defined the keep-out area, use [Tool]/[Auto Placement]/[Auto Placer] to auto-place the component. Once can define the constraint of the auto-placing.



Auto-placement is in progress

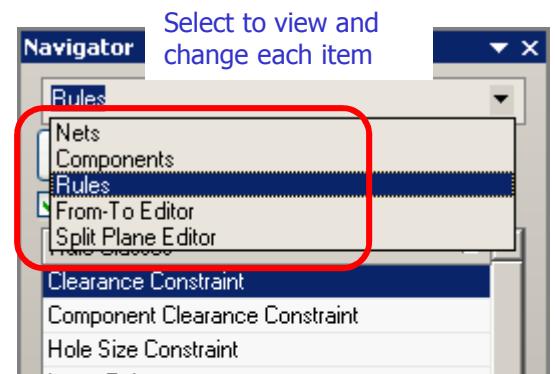
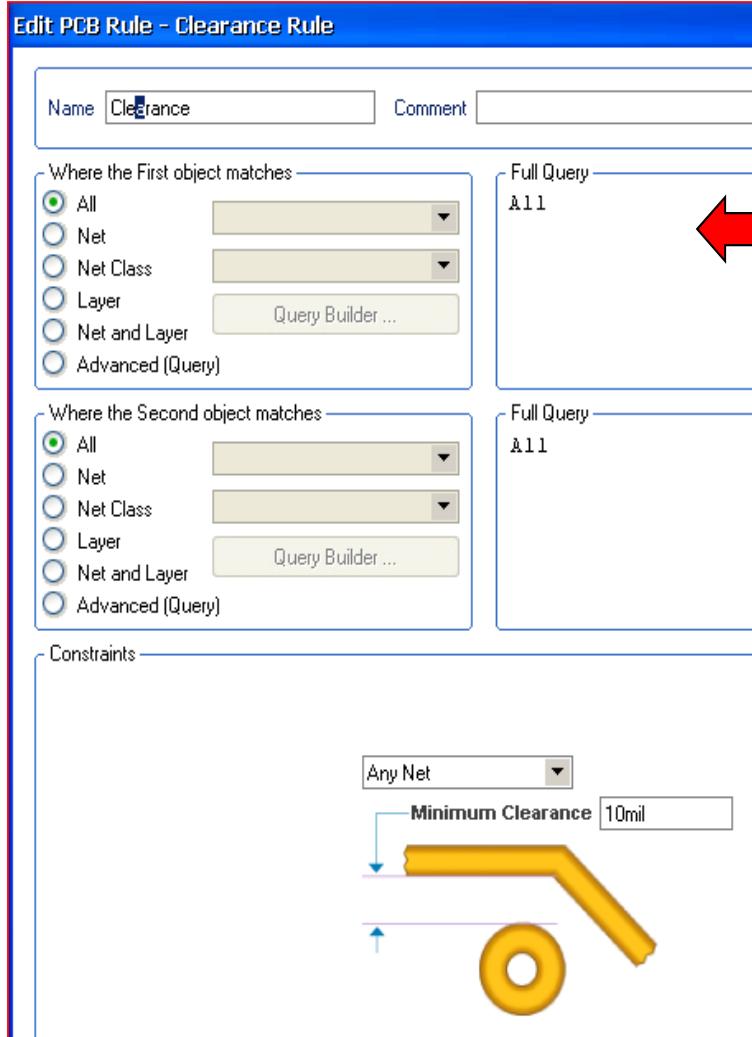
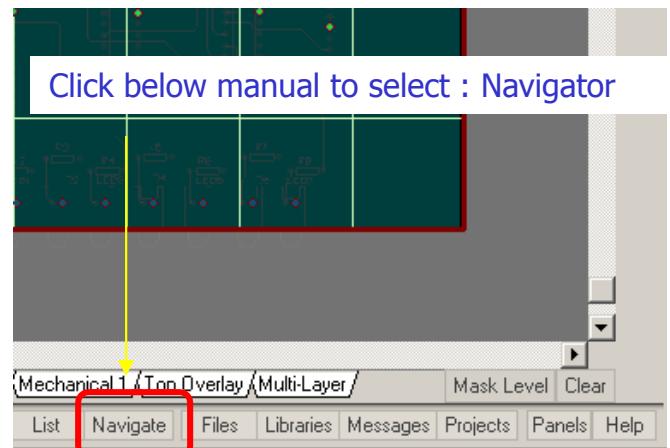
All components are within the keep-out area

Status bar indicate the progress

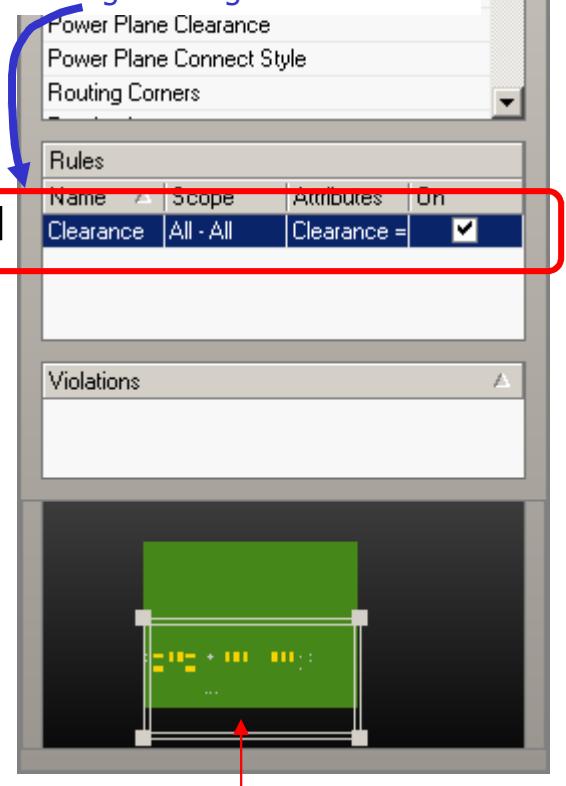


See a component or net on a PCB

Use Navigator



Double click to show detail setting and change setting



Position a PCB for viewing

[View]/[Fix Board] - VF

[View]/[Fix Sheet] - VH

[View]/[Fix Document] - VD

Important

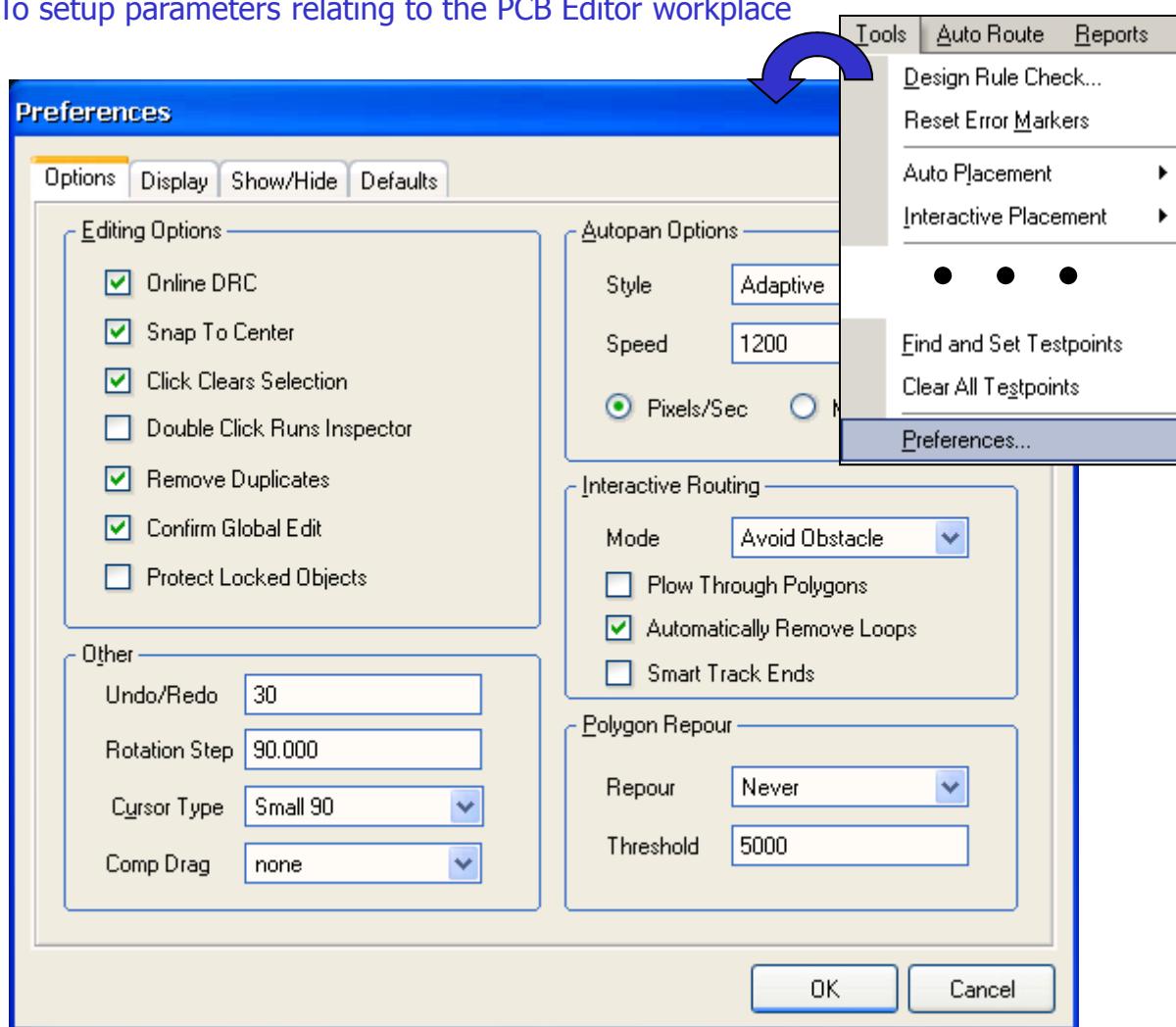


Magnify a area for viewing

[View]/[Area] - VA

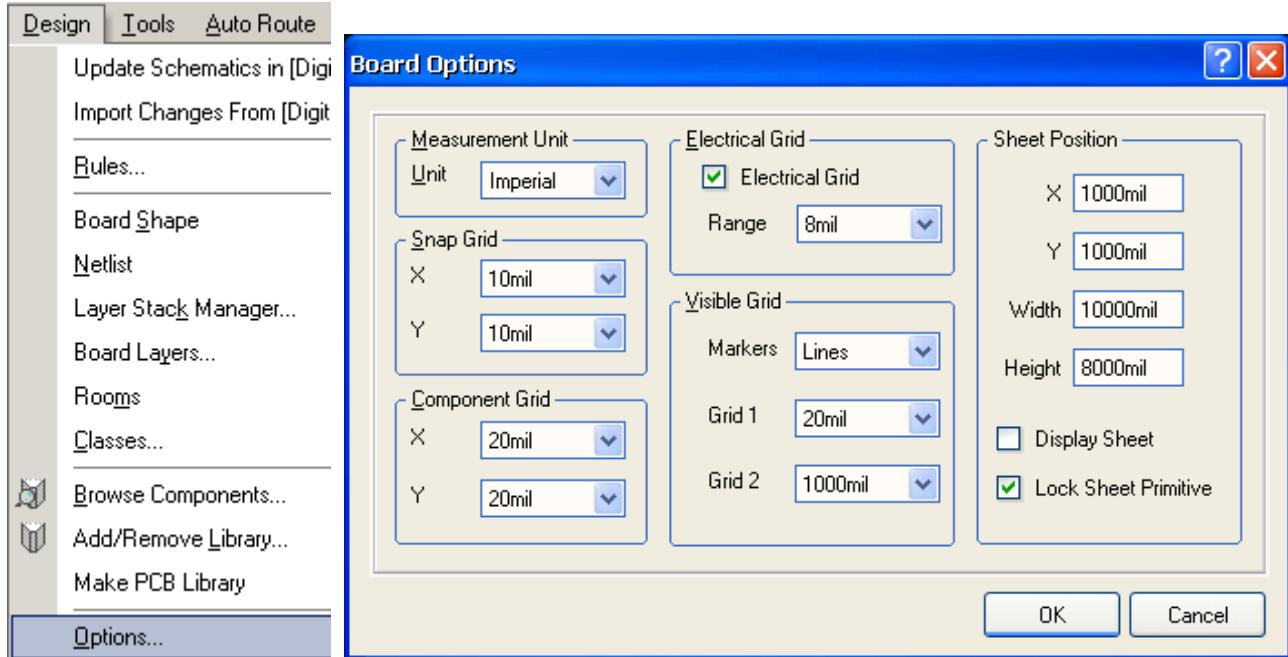
Preference Dialog

To setup parameters relating to the PCB Editor workplace



Design Setting

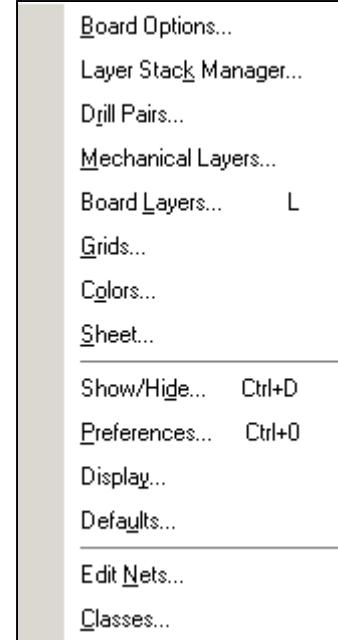
[Design] / [Option]



Short cut key for setup option

Press a "O" will pop-up a manual

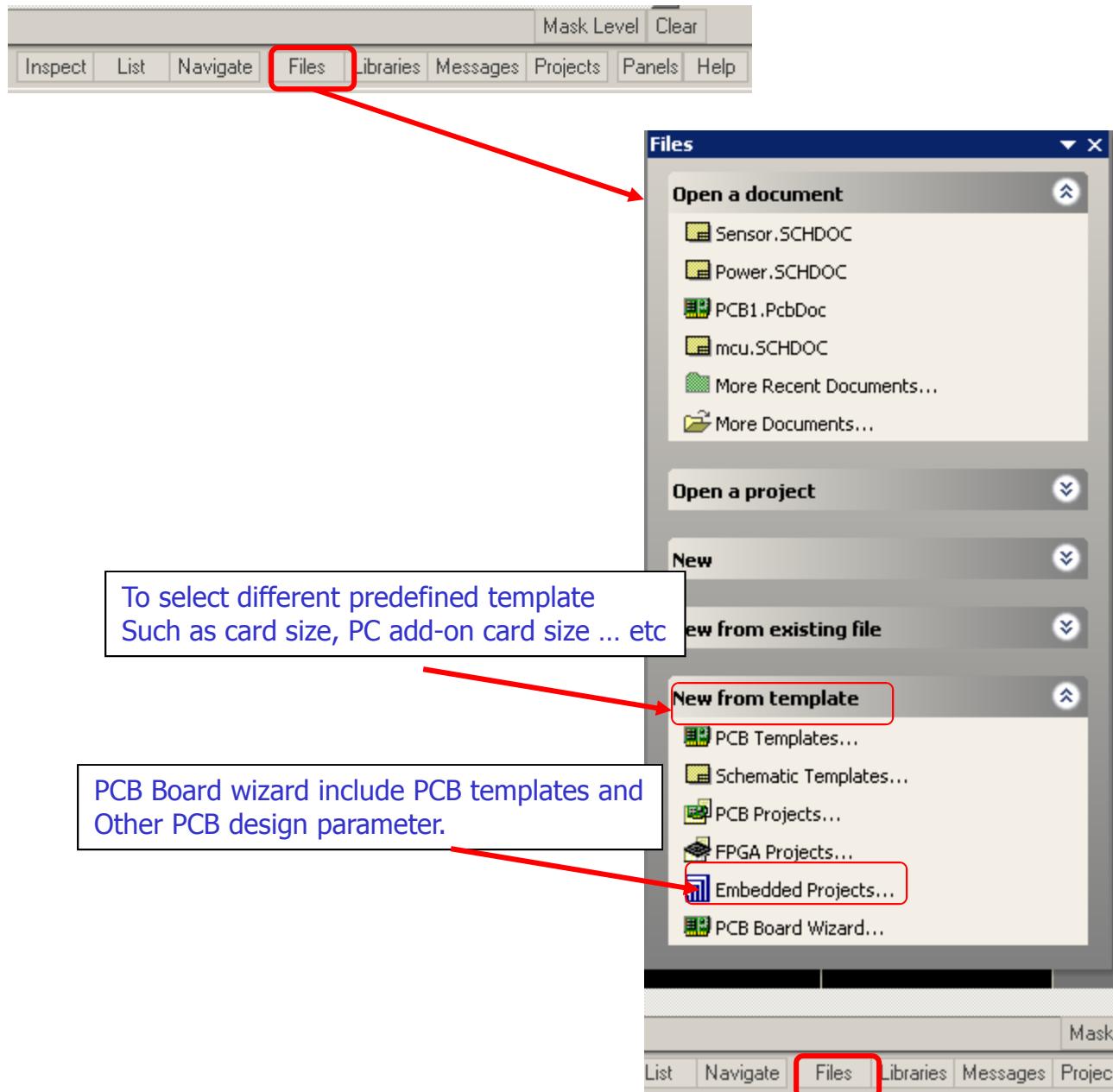
O →



Using PCB Template / Wizard to define a new PCB

Special FILE menu

The normal tool bar File menu is slightly different from the File menu from below

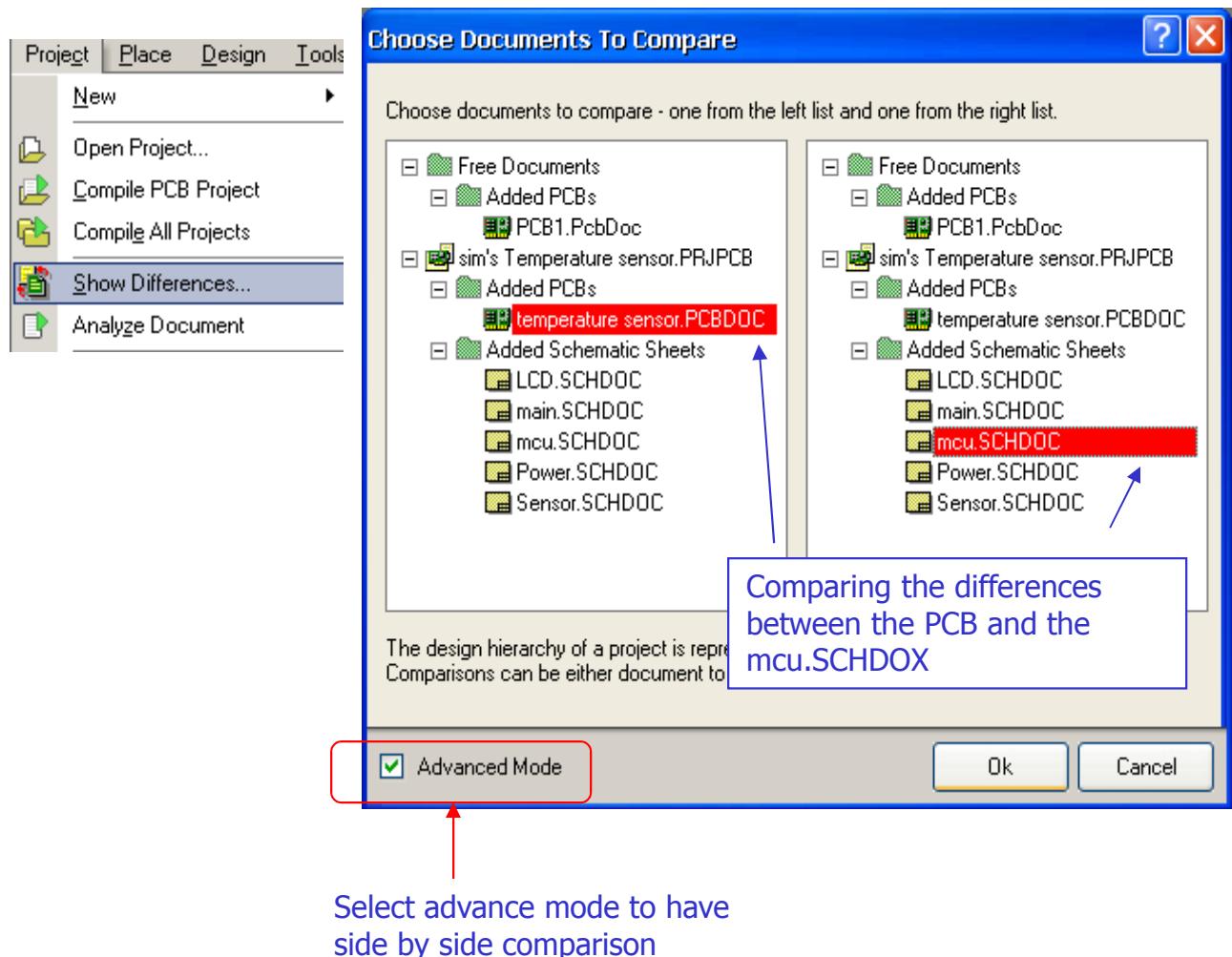


Resolve synchronization Error

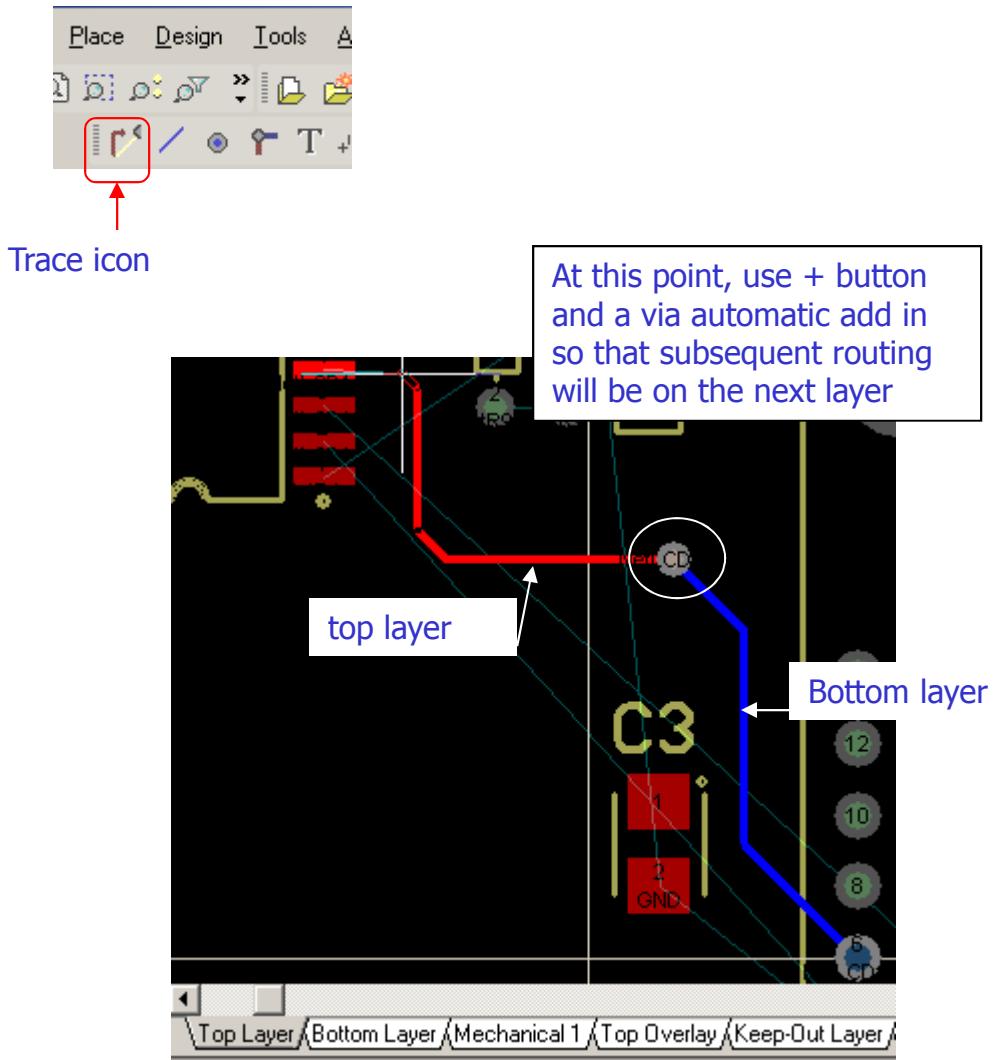
Two problems associate with Synchronization Error

- Missing component foot print information in schematic
- New foot print does not match old foot print. Pins on schematic symbol do not match the pads on the foot print

Show difference

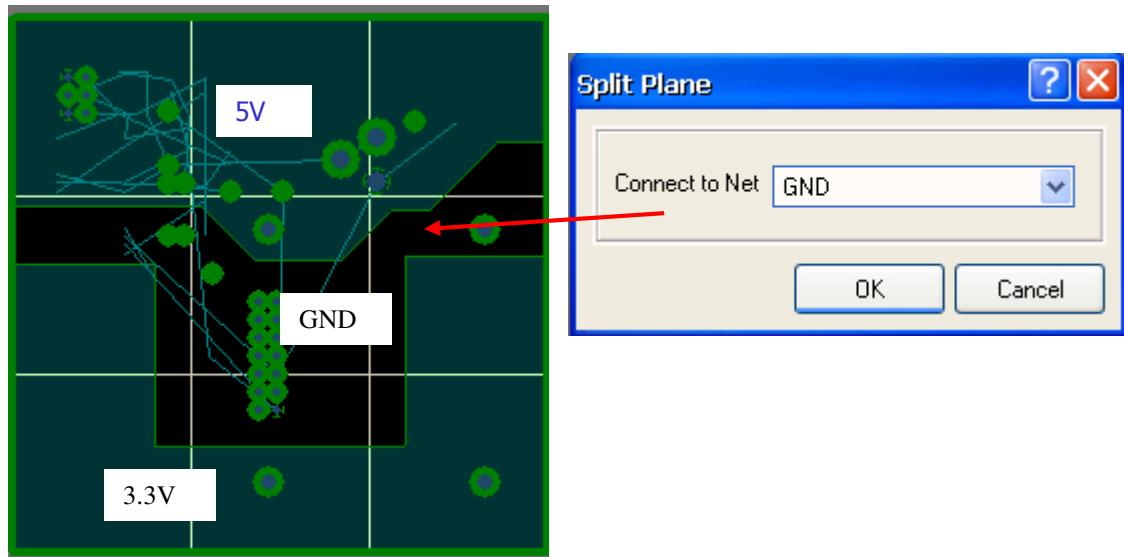


PCB Trace layout

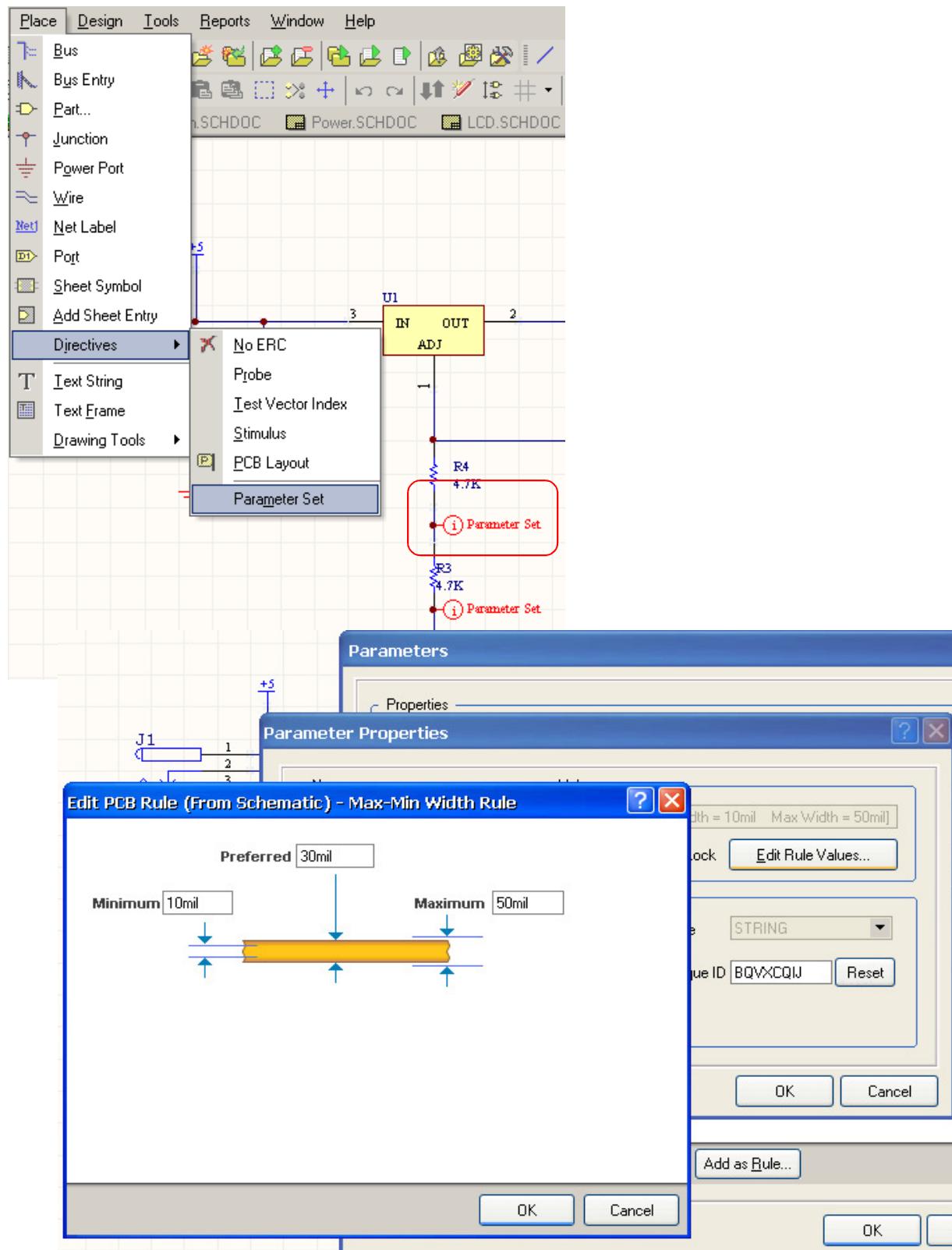


Split Power Plane

Internal planes can be split and shared amongst multiple nets.
Use line [Place] / [Line] to separate the plane into multiple regions
Define Net name connect to each plane

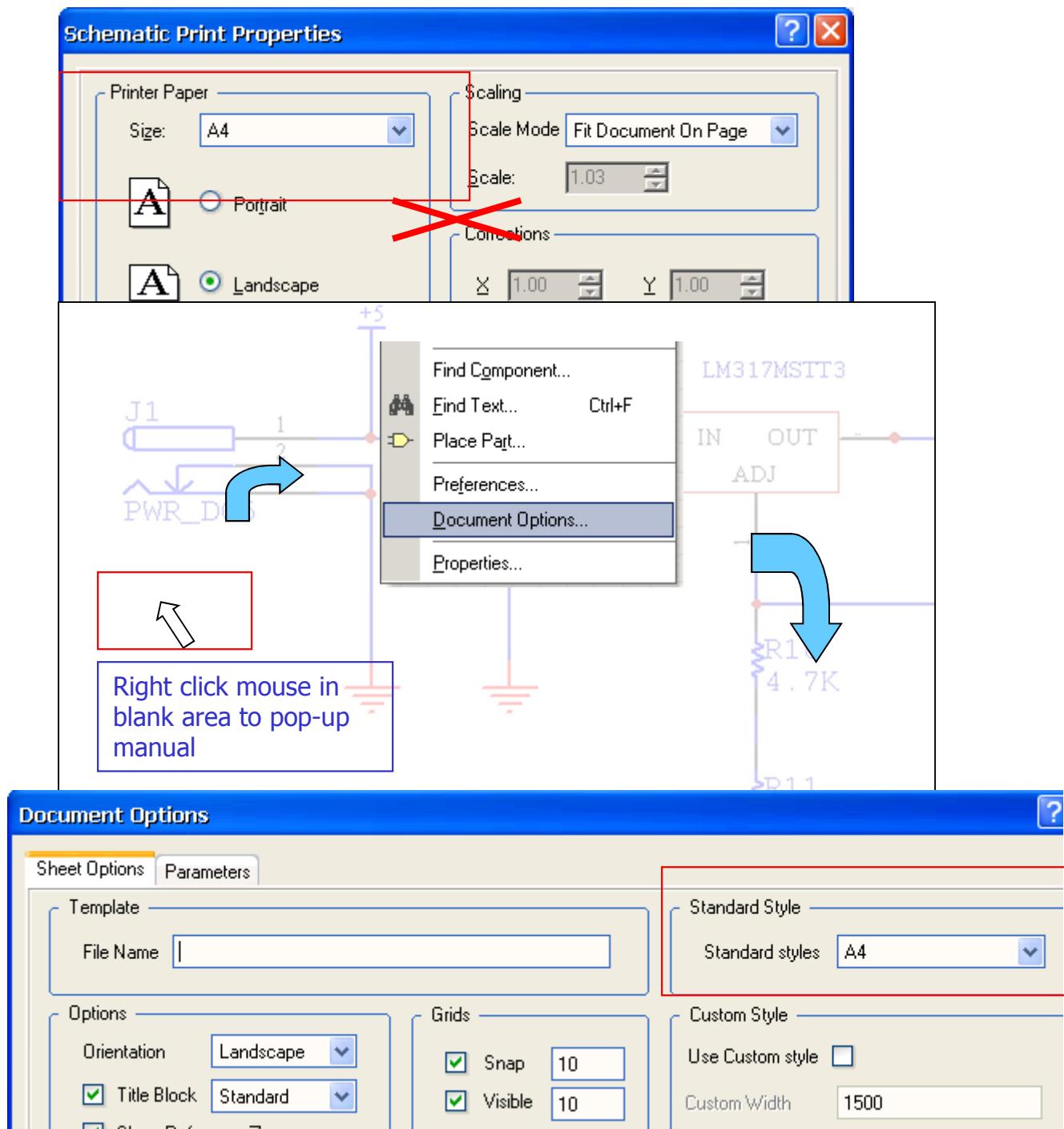


Specify a particular routing width on schematic



Print out a viewable hardcopy

In schematic sheet, your File/Page Setup may be in A4 size as shown below. But you have to make sure that your Document Setup is also in A4 size (NOT by default). Otherwise your print out may be too small



PCB Short cut commands

Measure Distance

CTRL + M and then select two points to get the distance

Layer Movement

- + next layer
- Previous layer
- * Next signal layer

L – display layer setup

G – set grid value

Q – Toggle units (Metric/imperial)

Rotate Component

ClickComponent +SpaceBar - rotate object anti-clockwise

ClickComponent + Shift + SpaceBar – rotate object clockwise

Display Size

PgUp – enlarge display size

PgDn – reduce display size

Shift + MouseRoller – enlarge/reduce display in smaller step

Move Parts

Shift + MouseLeft +Drag – move parts only, not connection

CTRL+ MouseLeft +Drag – move parts with connection

Toggle between Schematic and PCB

CTRL + TAB

(note : PCB and Schematic must be loaded inside the memory before execute this command)