High Speed PCB Design

Year 2003

Acknowledgement

Thanks to those people and websites that directly or indirectly contributed to this training material

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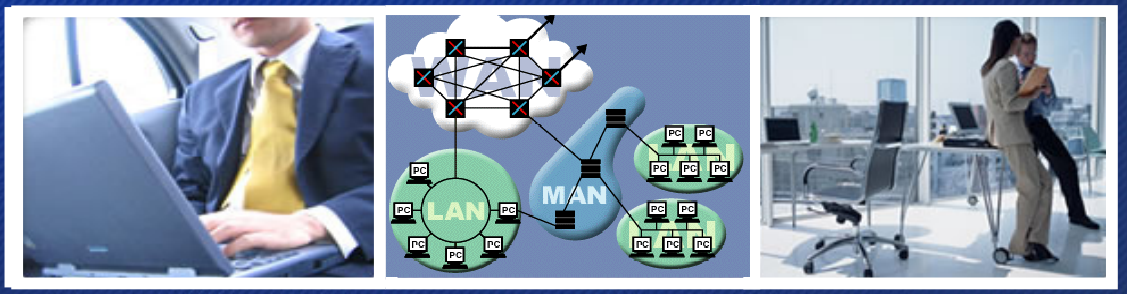

Topics to Cover

- High Speed Transmission – General
- Transmission Line Models
- Power and Ground Planes
- High Speed Signal Routing
- Signal Propagation
- Impedance Matching
- Power Supply Filtering
- Cross talk
- Ground Bounces

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High Speed Transmission

Questions for High Speed

Why special in high speed (high frequency) ?

How to design interconnection (routing) on PCB ?

How to reduce signal reflection (Impedance matching) ?

How to design power / ground planes ?

How to reduce EMI ?

How to design power bus ?

Ground bounce ?

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High Speed Transmission

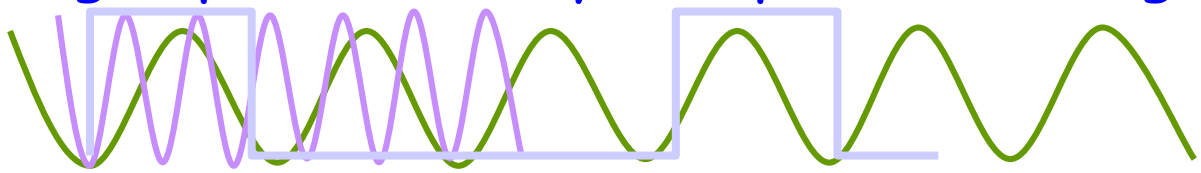
Low speed – low frequency response . Very little effect on signal

High speed – High frequency effect take over Transmission line characteristic

Short line can become

- Ringing
- Cross Talk
- Reflection
- Ground Bound

How high is high speed ? Very sharp rise time e.g. <10 nSec



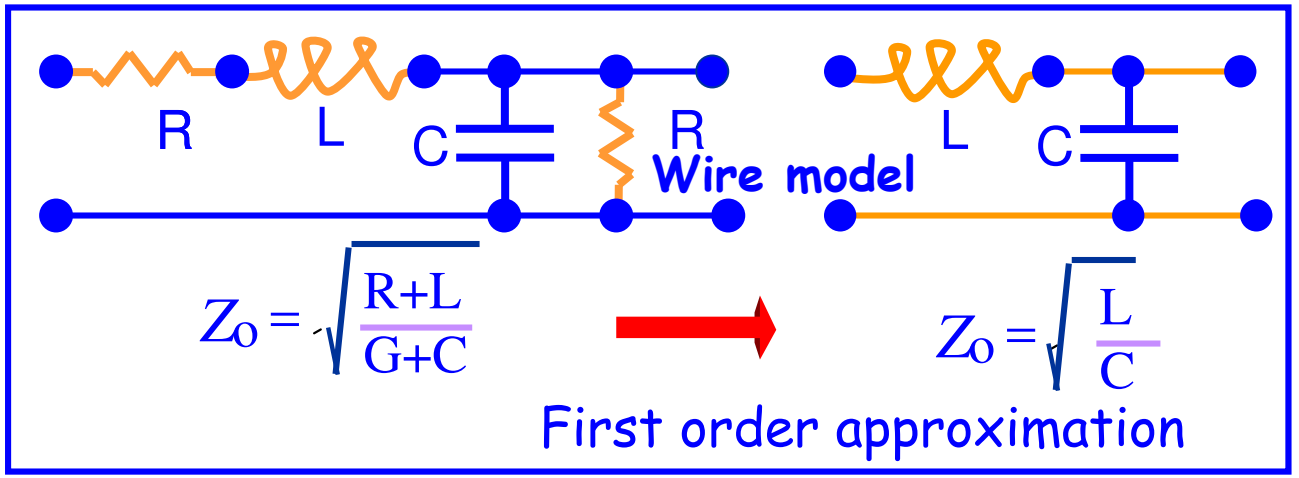
High Speed Transmission

High Speed Impact on System

- Digital properties
- Analog effect

At high speed digital signal transmission, shortest PCB trace suffers from transmission line effect. In high speed (high frequency) environment, we talk about

- Impedance
- Inductance
- Capacitance



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High Speed Transmission

Transmission Loss

Dielectric Absorption

High frequency excite molecule in the insulator

→ Absorb signal energy

→ Reduce signal strength

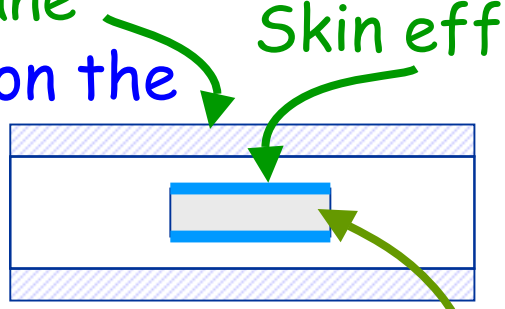
PCB material, wire/cable insulator

Skin Effect

High frequency signal tend to travel on the conductor's surface

→ Reduce conductive area

→ increase of resistance , more attenuation



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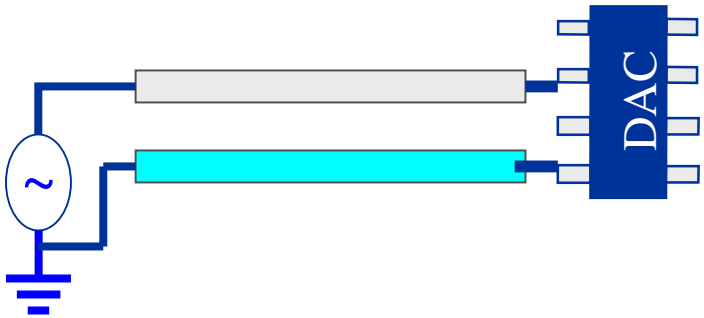
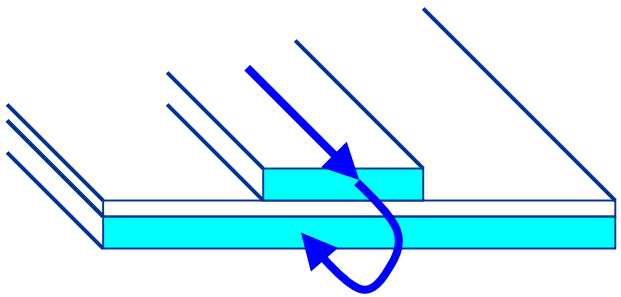
High Speed Transmission

Signal Return Path

- Every signal line (PCB or cable) must have return path close to it





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Transmission Line Models

Transmission Line Models

Parameters

Dimension in mil (milli-inch)

Zo in ohms

L in nH/in

Co in pF/in

Tpd in nSec/in

1 oz copper,
T = 1.4 mil thickness

FR4 Fiber gloas Epoxy	Er = 4.7
Teflon	Er = 2.2
Teflon Glass	Er = 2.5
Polyimide	Er = 3.5
Polyimide Glass	Er = 4.2

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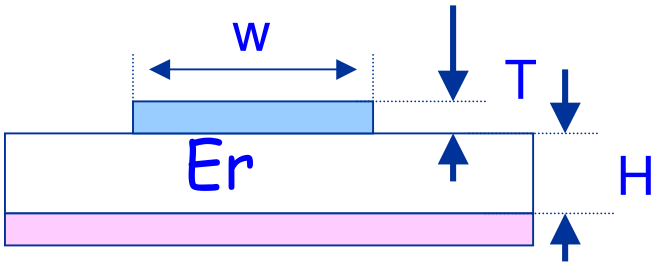
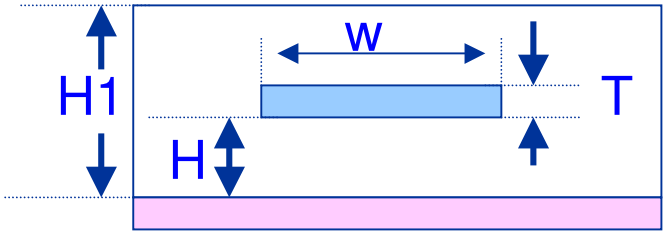
Transmission Line Models

Microstrip



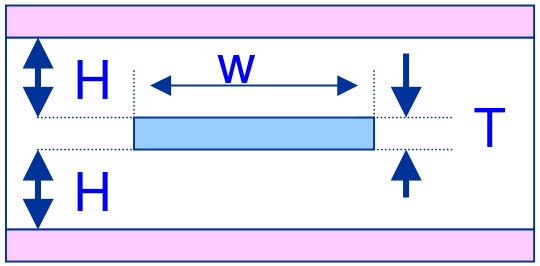
Er' = Er x (1 - Exp ((1.55 x H1) / H)))
Tpd = 0.0833 x (1.016 x SQRT (Er'))

Embedded Microstrip



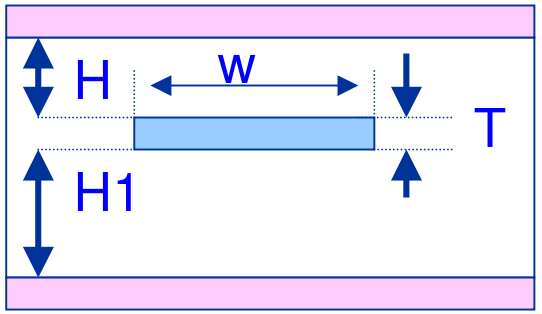
Er' = Er x (1 - Exp ((-1.55 x H1) / H)))
Tpd = 0.0833 x (1.016 x SQRT (Er'))

Stripline (Symmetic)



Tpd = 0.0833 x (1.016 x Sqrt (Er))

Stripline Asymetry



Tpd = 0.0833 * (1.016*(Sqrt(Er)))

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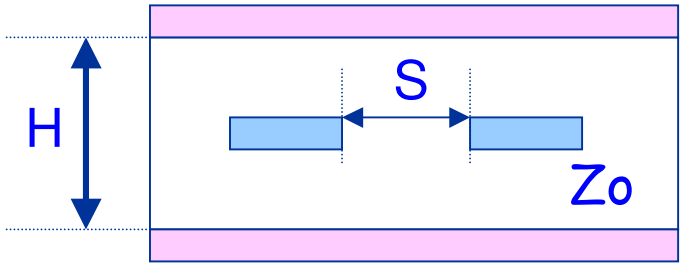
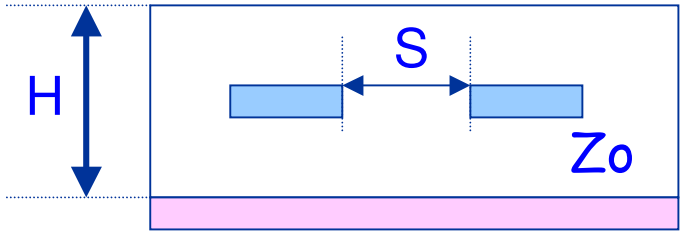
Transmission Line Models

Differential Stripline



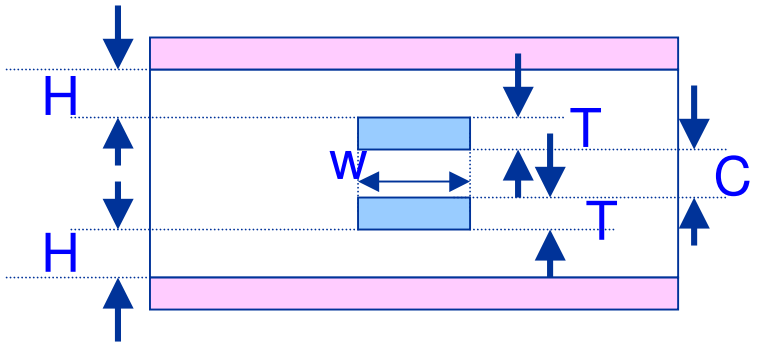
Zdiff = 2 x Zo (1-
0.347 x Exp (-2.9 x (S / H))))

Differential Microstrip



Zdiff = 2 x Zo (1
-0.48 x Exp (-0.96 x (S / H))))

Dual Stripline



Tpd = 0.0833 * (1.016 * (SQRT(Er)))

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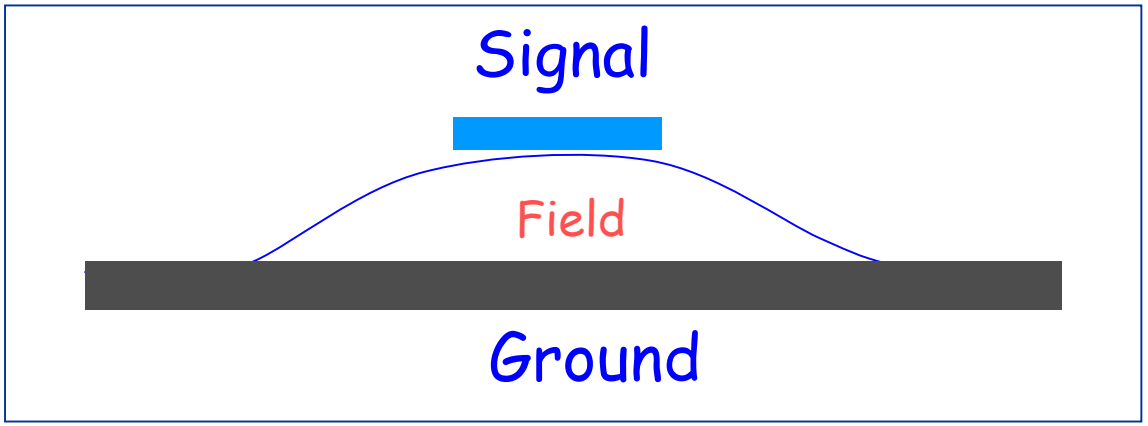
Power and Ground Planes



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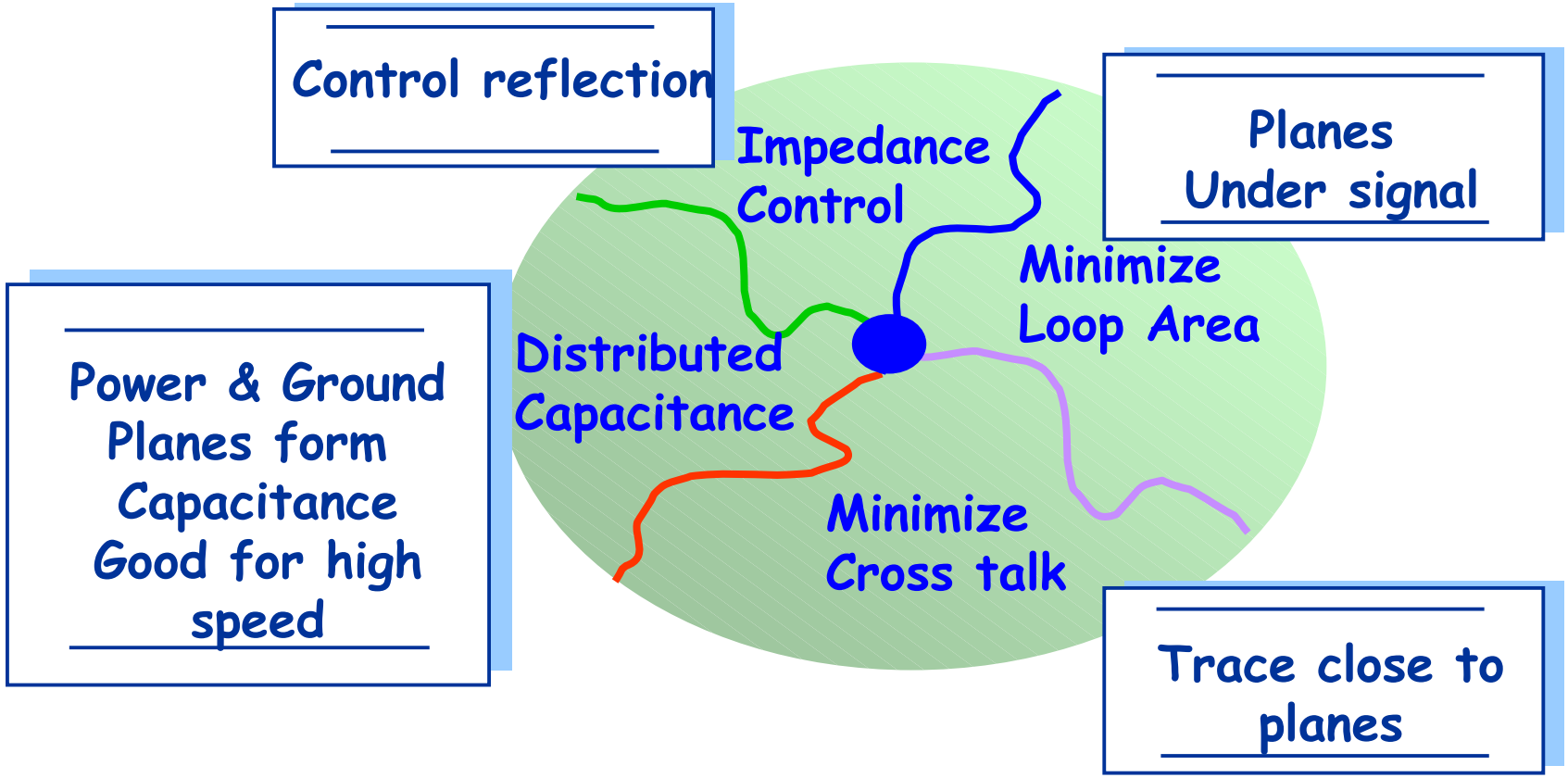
Power and Ground Planes

- DC voltages in a system : 5V, 3.3V, 2.5V, 1.8V, 1.2V
- Lower voltage : power saving and faster (dV/dt smaller)
- Multiple power supply : noise isolation



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Power and Ground Planes

- Different voltage planes should Not
  - overlap each over (noise coupling)
  - sharing same ground plane (noise coupling and ground bounces)
- Sensitive to nose ?
  - Use separate voltage plane and ground plane
  - All ground planes need to star connected to a single point ground (power supply's ground)
- PCB Cost is key concerned & noise is not a issue ?
  - all the power supply planes can reference to a single ground plane

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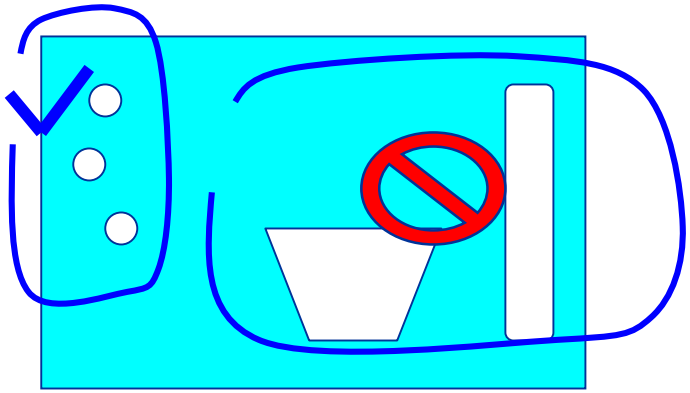
Power and Ground Planes

Plane Discontinuity

- High speed design need solid ground/power planes
- Via / through hole create holes in planes but effect minor
- Slot / Void create big empty space in planes causing major problems :
  - Signal impedance mis-match
  - longer high speed signal return path(EMI problem)



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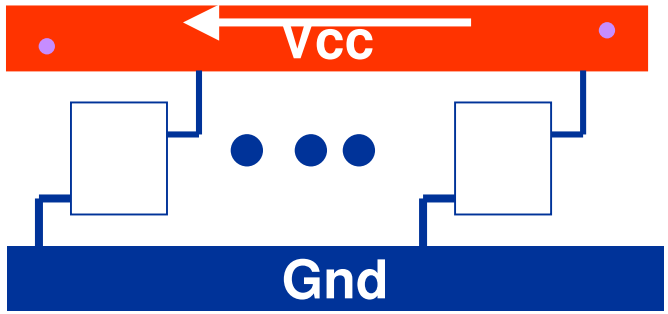
Power and Ground Planes

Vcc Voltage Drop

- When design power bus with many devices drawing high current , Voltage drop is significant even With small resistance across the Power bus



No more margin for voltage

I_{Total} = 2A

R = 0.125 amp

V_{drop} = 0.25 v 5V +/- 5%

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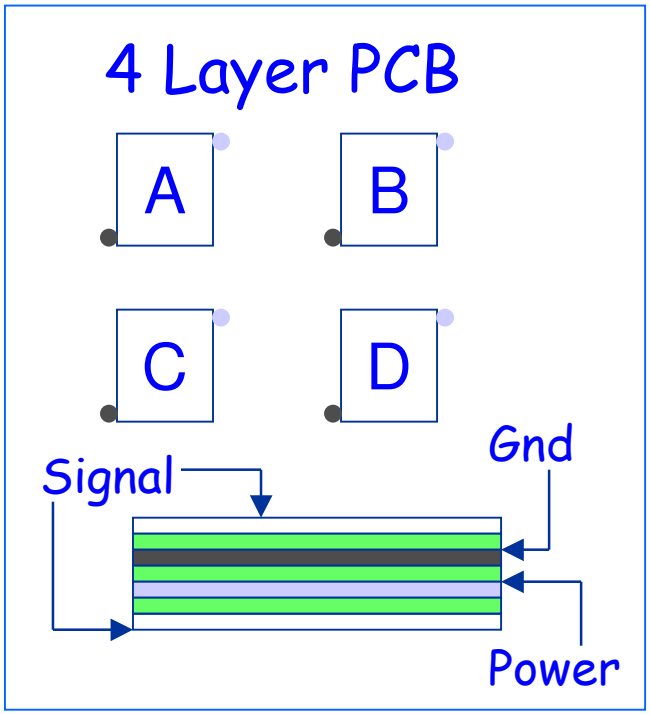
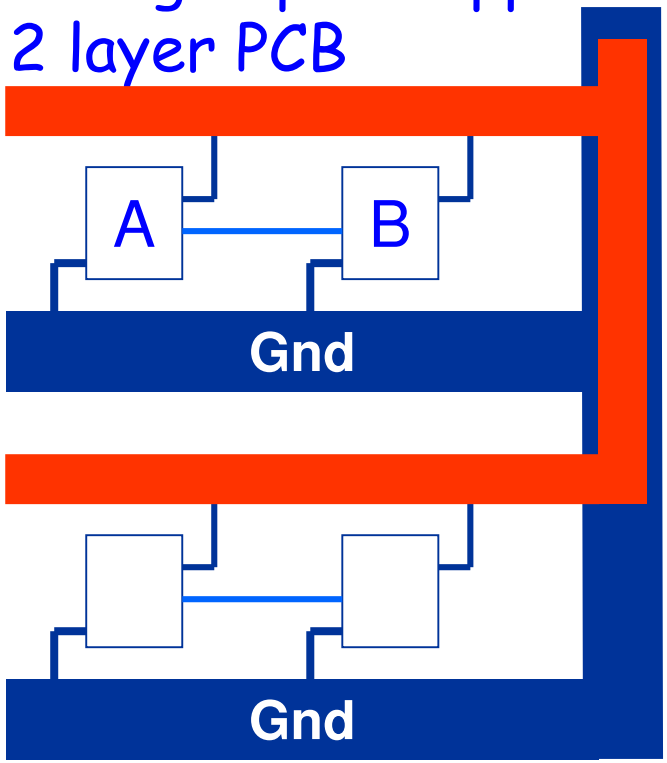
Power and Ground Planes

4 and 2 Layer PCB



Noise generated are distributed

Non high speed application - 2 layer PCB



Noise generated by device A Will couple into device B

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High Speed Signal Routing

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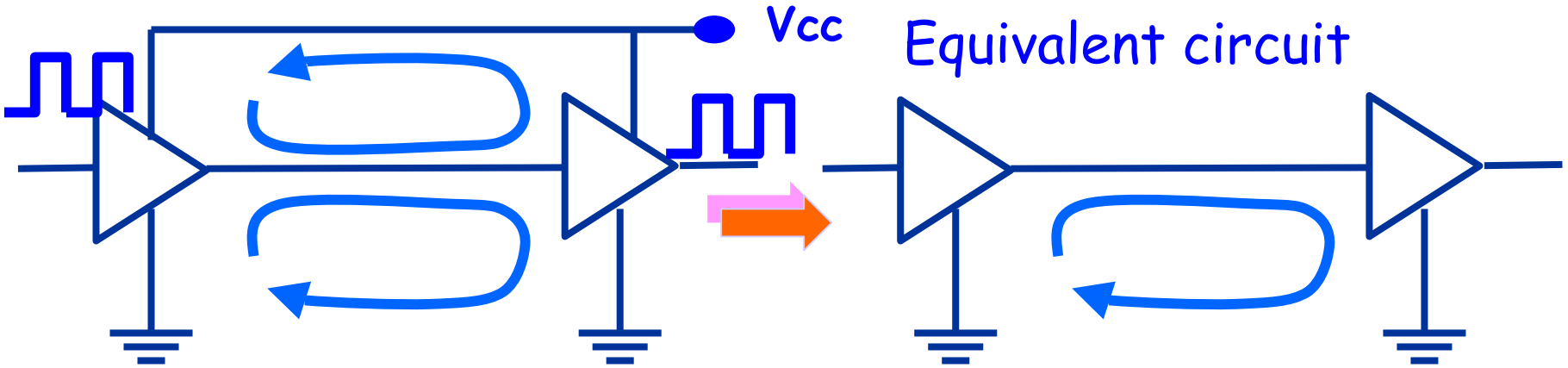
High Speed Signal Routing

Signal Return Path



2 Possible current loop

- AC return signal take the path of least impedance (not necessary least resistance) to current

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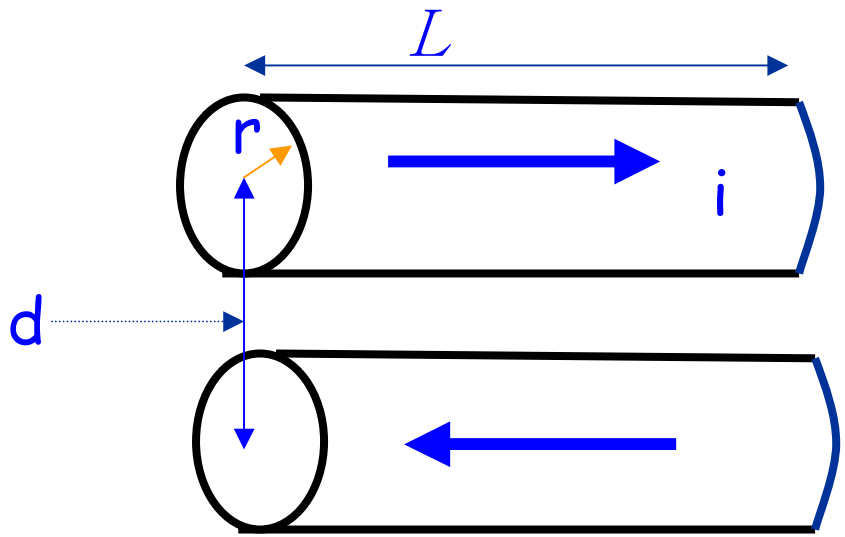
High Speed Signal Routing

- At high frequency (speed) , impedance increased with inductance
- Least inductance path is the path in the plan directly under the signal path



$L = k\,L \ln((d-r)/r)$

d ↑ L ↑

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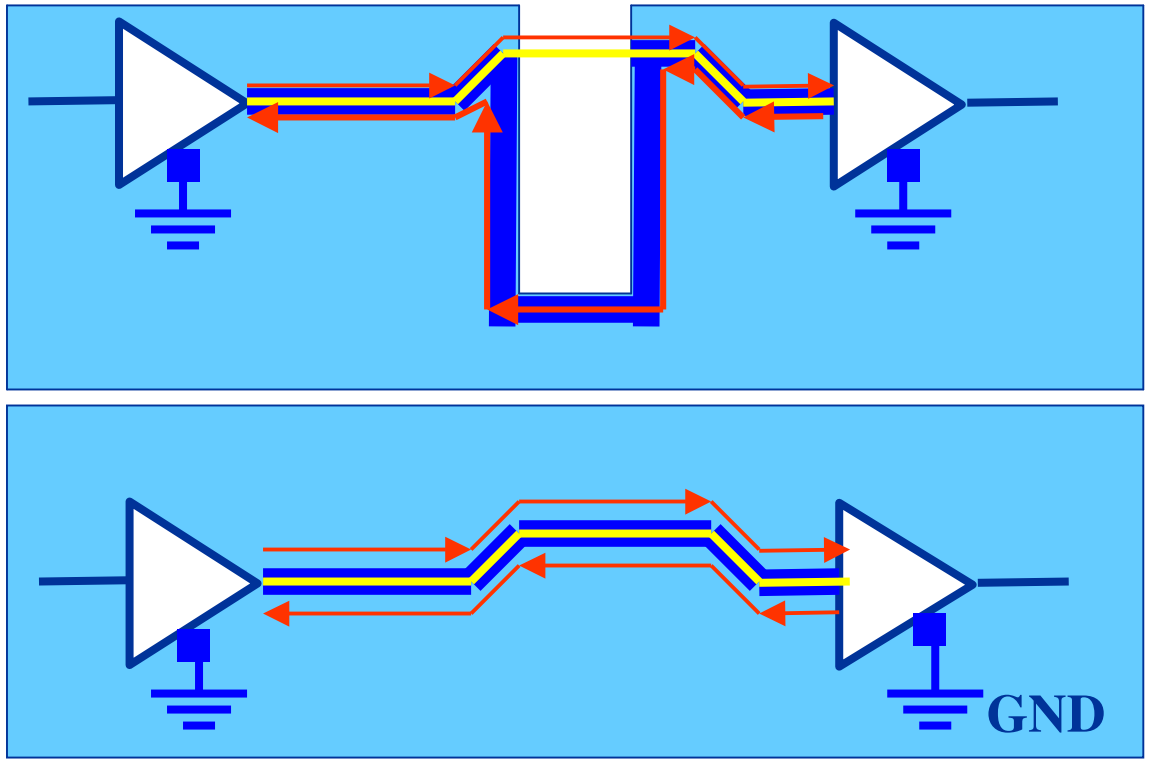
High Speed Signal Routing

Slotted / Complete Ground Plan

- As speed increases, signal return path directly underneath the signal trace (Gnd/Pwr planes)



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High Speed Signal Routing

Digital & Analog Ground Planes

- Digital circuit generate high noise
- High speed analog circuit sensitive to noise
- Digital and analog ground planes need to be separated
- Both ground plan are tied together at the system power supply ground
- For a DAC device ,the converted analog signal line need to go into the analog circuit, where is the return path ?
- Place a bridging path between the two ground plan under the signal line

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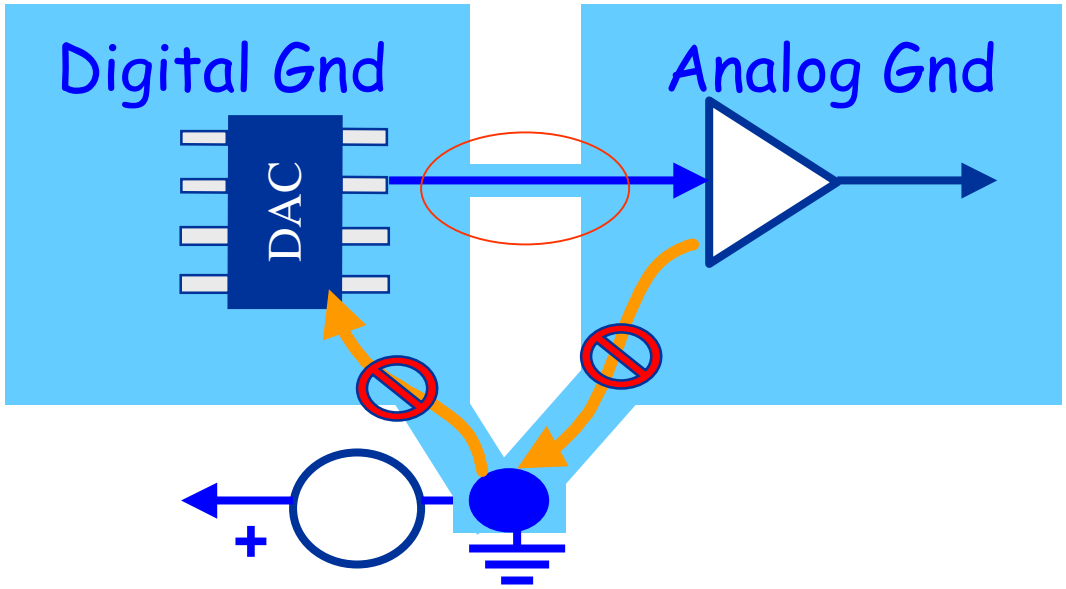
High Speed Signal Routing

Combine Digital & Analog Ground Planes



Ground plane under the signal line that need to go across the Digital and analog section

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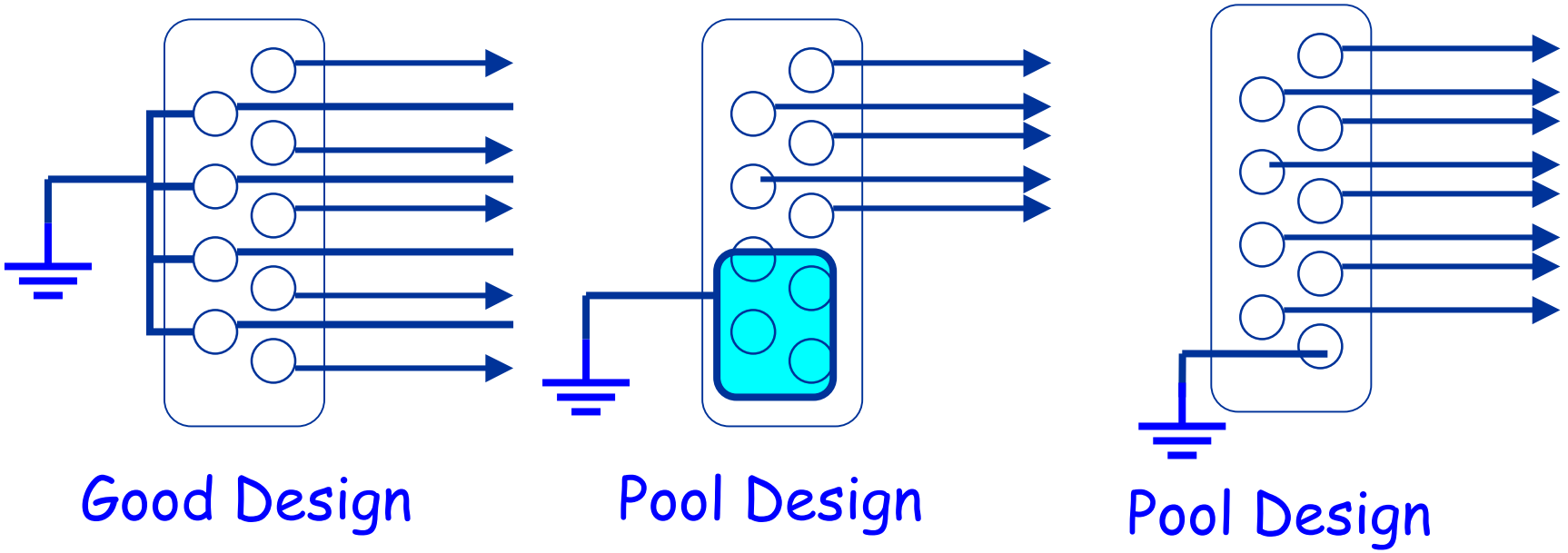
High Speed Signal Routing



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High Speed Signal Routing

Clock Signal

- Avoid serpentine routine (as straight as possible)
- Avoid travel in multi-layers
- Avoid via in clock transmission
- Route in microstrip, Er = 1
- Ground plan next to outer (signal) layer to minimize noise
- Sand wish the clock layer by ground plan if it is in the inner layer
- Terminate clock signal

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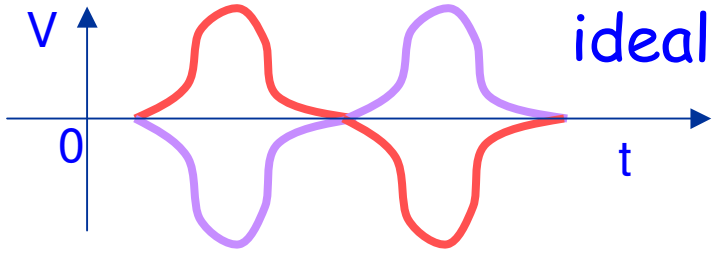
High Speed Signal Routing

Differential Signal

- Two signal wires compliment each other
- Good for low signal level application v+ - (v-) = 2v
- Perform better than single ended in noisy environment
- Crossover theoretically at 0 v
- If return for one signal (+) is exactly equal to the other signal (-), the sum is zero and no current flow
- If the sum is not zero, the resultant current have to flow to ground



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High Speed Signal Routing

Design rules for differential signal

- Differential trace must be equal length
  - with equal length, the cross over point the can be zero
- Route differential traces closely together
  - minimize current loop (reduce EMI)
  - noise coupled on both traces will be more equal and thus cancel each other
- Constant separation between traces for entire length
  - impedance remain constant

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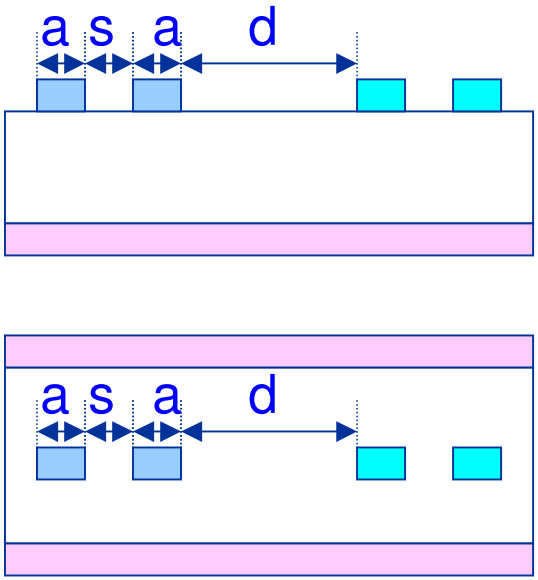
High Speed Signal Routing

Differential Signal



- D > 2S
- S – as small as possible
- Constant distance and same length between differential Trace
- Minimize impedance mismatch and inductance and avoid via

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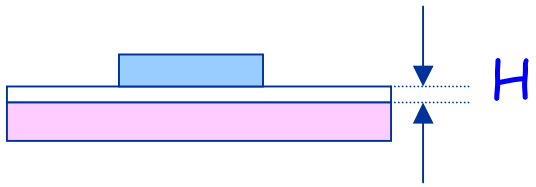
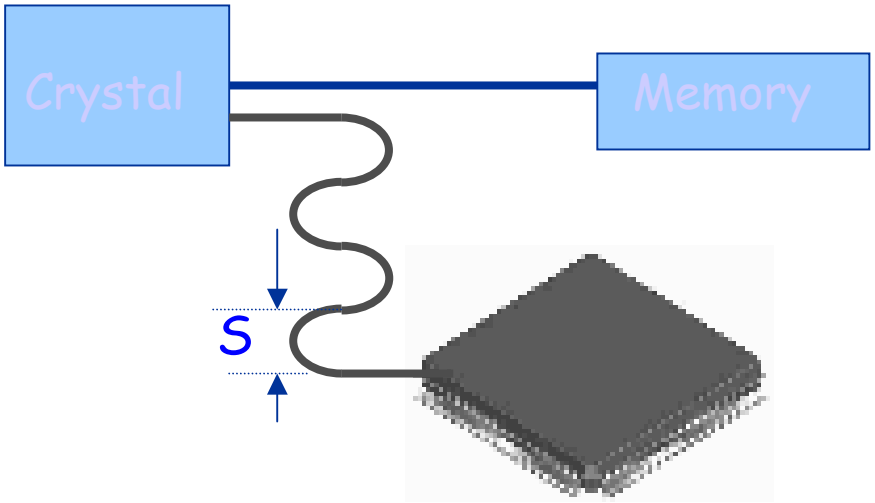
High Speed Signal Routing

Equal Length

- Trace length matching when a source need to drive multiple loads with same length
- S >> 3H, avoid serpentine for clock





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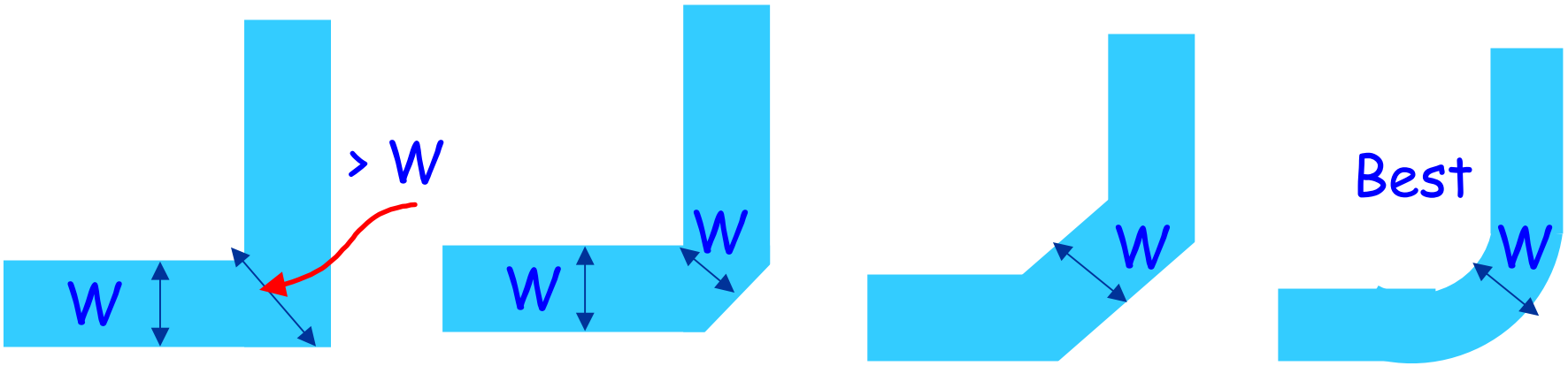
High Speed Signal Routing

Turning of Trace

- Incorrect turning of signal traces changes it dimension and thus Zo which causes reflection, distortion and noise
- E field becomes concentrated at the sharp corners causing emission



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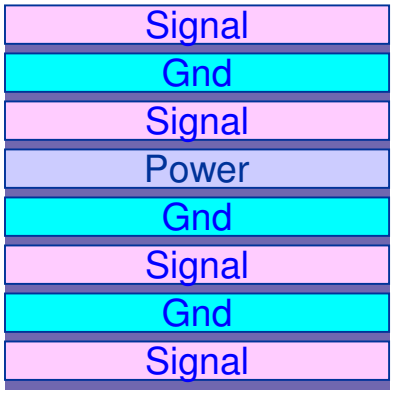
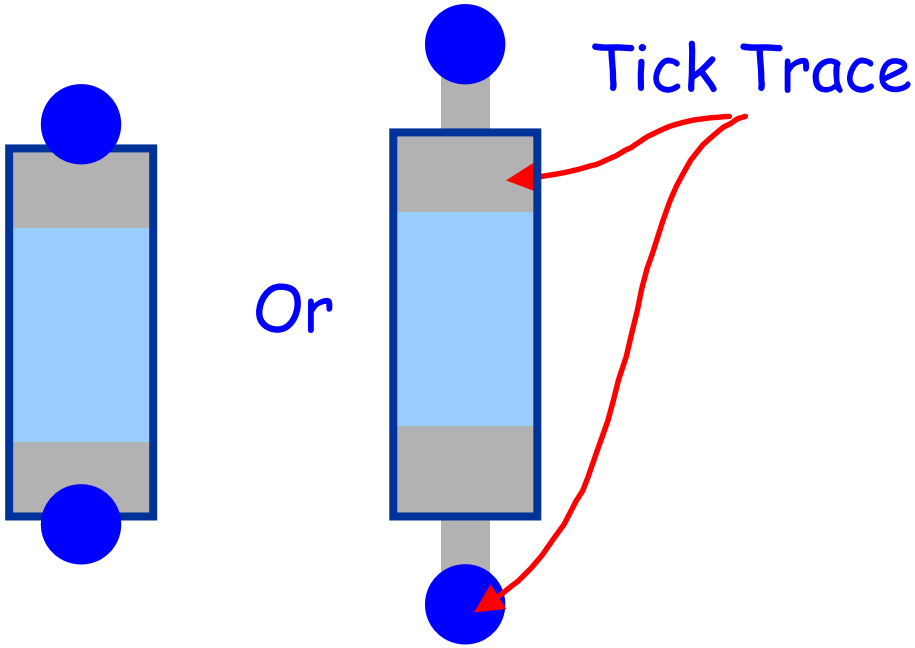
High Speed Signal Routing

Misc

8 Layer PCB





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Signal Propagation

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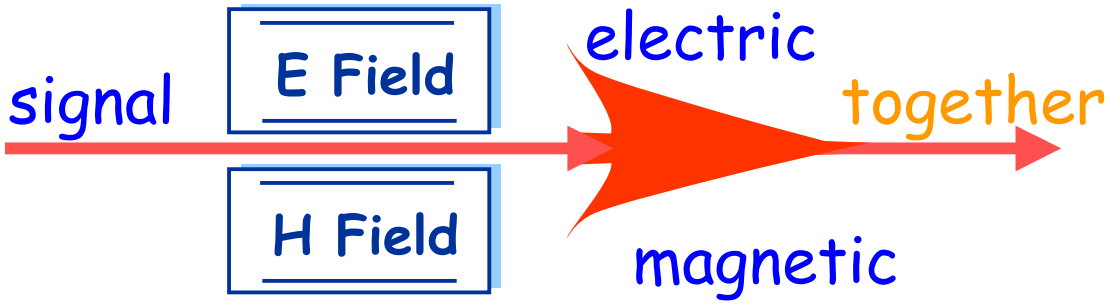
Signal Propagation



- It is not how fast electrons travel in copper
- It is how fast the electromagnetic field can travel in the medium that it is in
- Electromagnetic wave travel at the speed of light in vacuum. But slower in medium
- In FR4, signal travel at 6" per nsec

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Signal Propagation

- When signal line > transition time of a signal by 4 times

Tr (ns)	Line Length (in)
5	> 8.6
4	> 6.9
3	> 5.1
2	> 3.4
1	> 1.7

- Tr = 1 ns, Critical length = 3" – verified ?

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Impedance Matching

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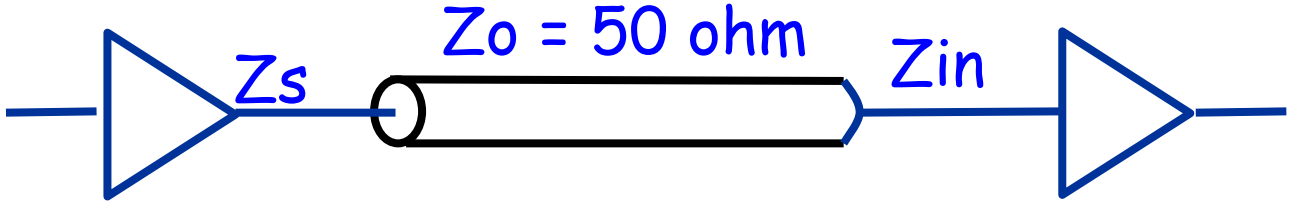
Impedance Matching



If Zs ≠ Zo ≠ Zin → Mis Match

Mis match

- Overshoot
- Under shoot
- Ringing
- Stair step waveform
- Possible digital error

Why ?

Transmitted signal is not fully absorbed by receiver and excess energy is reflected back to transmitter, back and forth till the signal dies off

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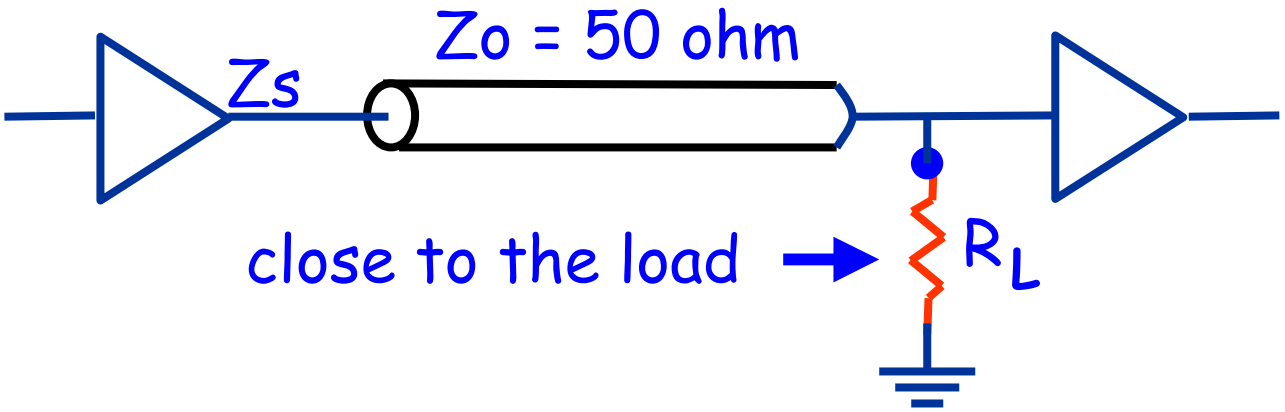
Impedance Matching

Parallel Termination



- Cause loading to the driving source

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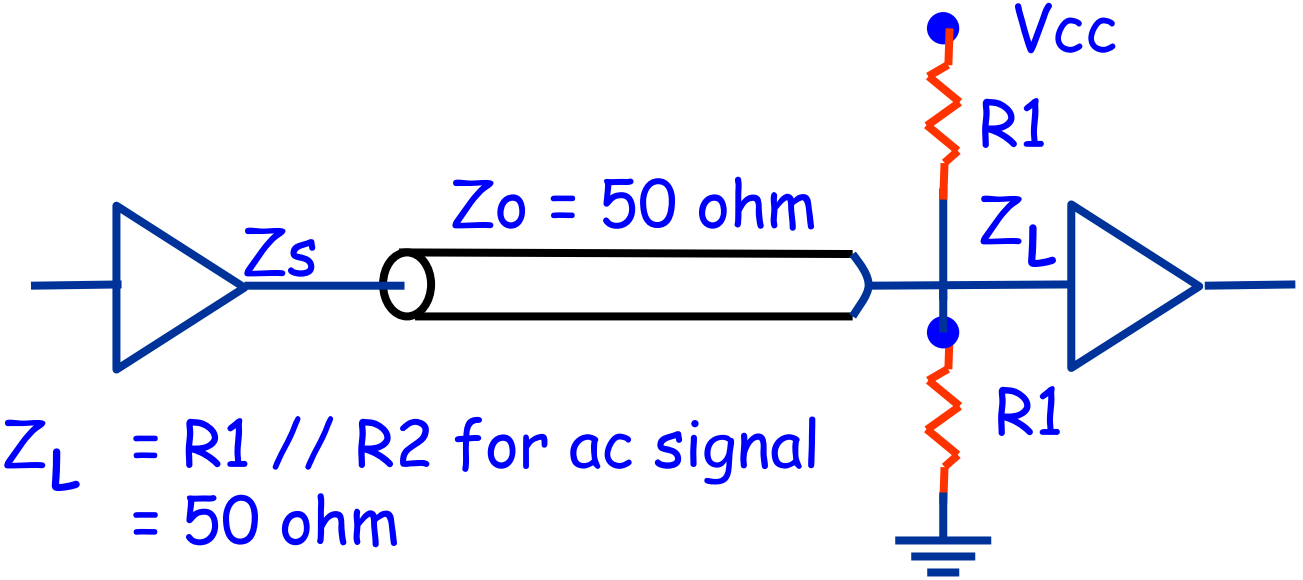
Impedance Matching

Thevenin Parallel Termination



Z_L = R1 // R2 for ac signal
= 50 ohm

- Reduce current load on driving source
- Consume DC current from Vcc

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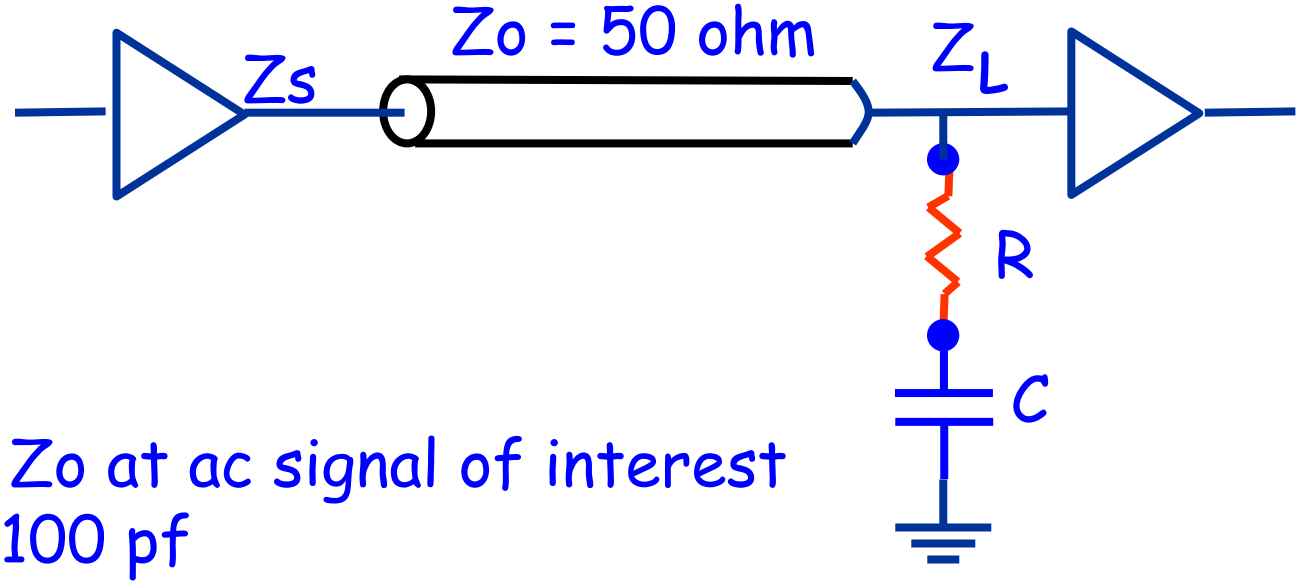
Impedance Matching

Series RC Termination



- R = Zo at ac signal of interest
- C > 100 pf
- C block DC low frequency signal while passing high frequency signal

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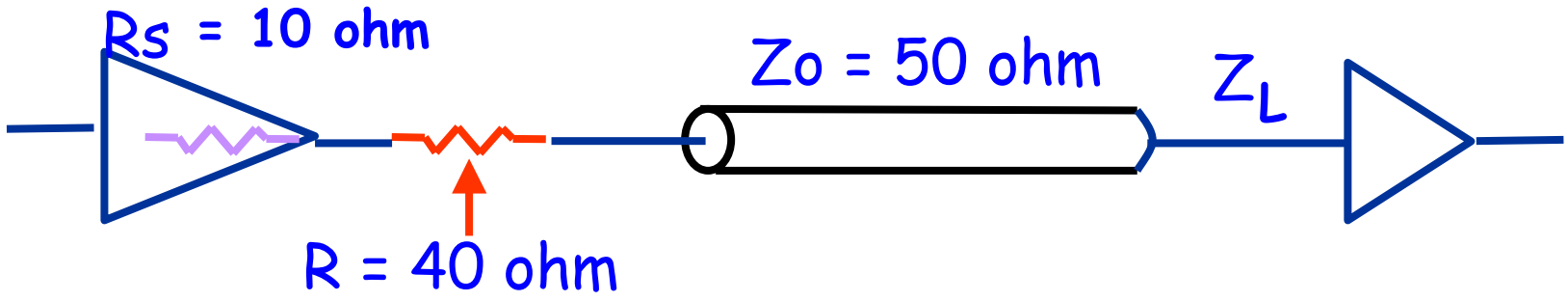
Impedance Matching

Series Source Matching



- Match impedance at signal source
- Add series resistance to Rs to match the line signal source Zo
- Attenuate secondary reflection
- Delay signal path as it increase RC time constant

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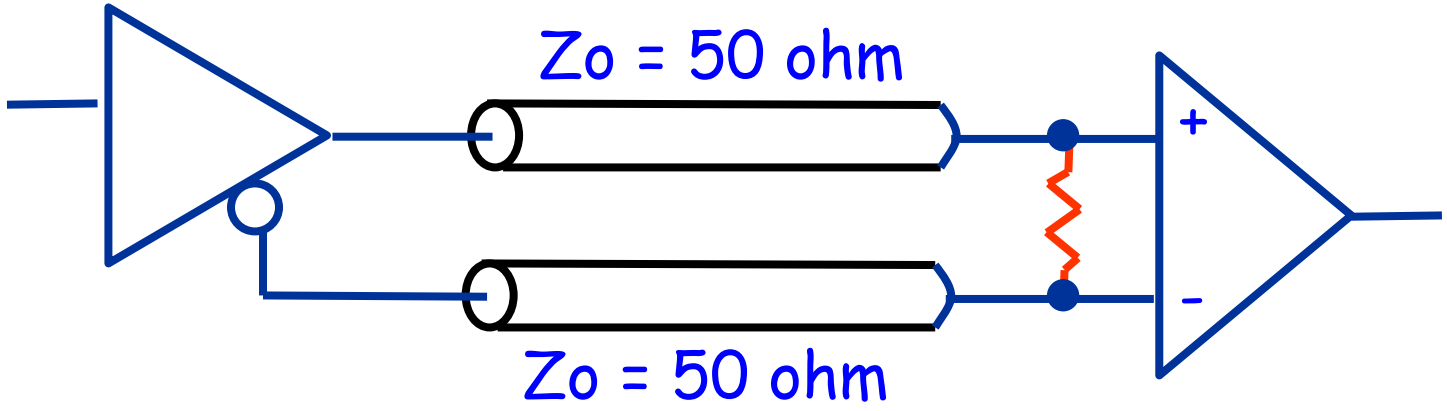
Impedance Matching

Differential Pair Termination



- Each signal path Zo = 50 ohm to ground
- Total $Z_{\text{Differential pair}}$ = 50 + 50 = 100 ohm

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Power Supply Filtering

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Power Supply Filtering

Decoupling Capacitors

Electrolytic
Low Frequency

- Supply extra Switching Current
- Filter low frequency noise (e.g. 60 Hz)
- Electrolytic – 10 uF to 100 uF

Ceramic
High Frequency

- Filter high frequency noise > 100 MHz
- Ceramic – 0.01 uF to 0.1 uF

Power Plan & Ground plan for distributed capacitance

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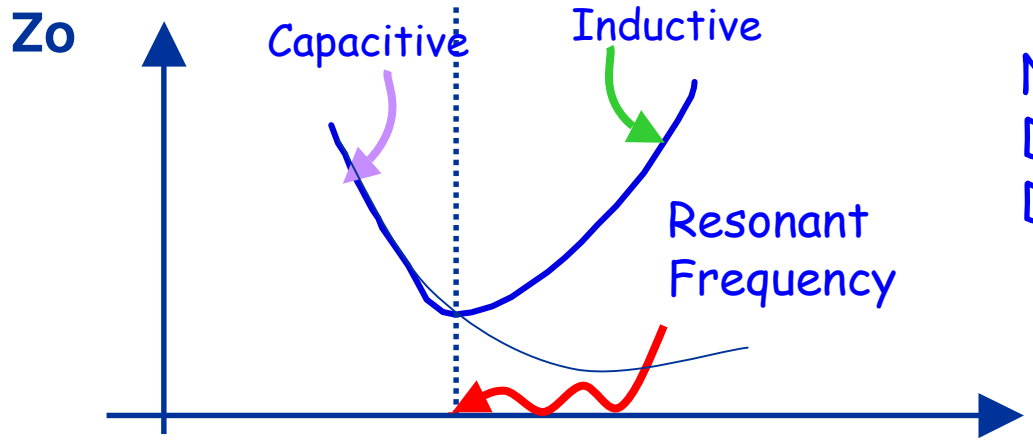
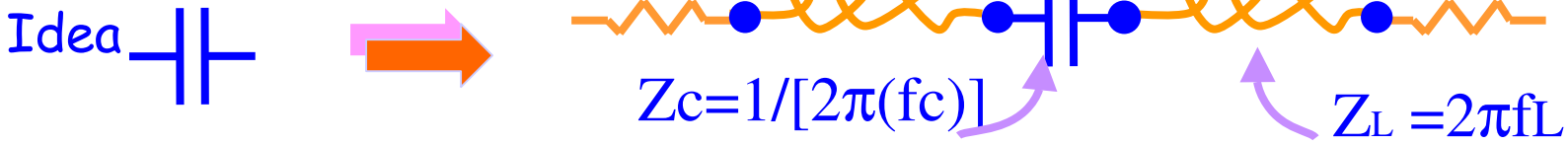
Power Supply Filtering

Decoupling Capacitors



Need combination of Different types of Decoupling capacitor



At high frequency, parasitic component, (R,L) become significant. Beyond resonant frequency, capacitor no more behavior as idea capacitor

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Power Supply Filtering

Capacitor

Electrolytic

- ❑1uF to 100 uF
- ❑Power supply bus

C0G

- ❑< 0.1 uF
- ❑Use in noise sensitive device
- ❑In parallel with Ceramic chip

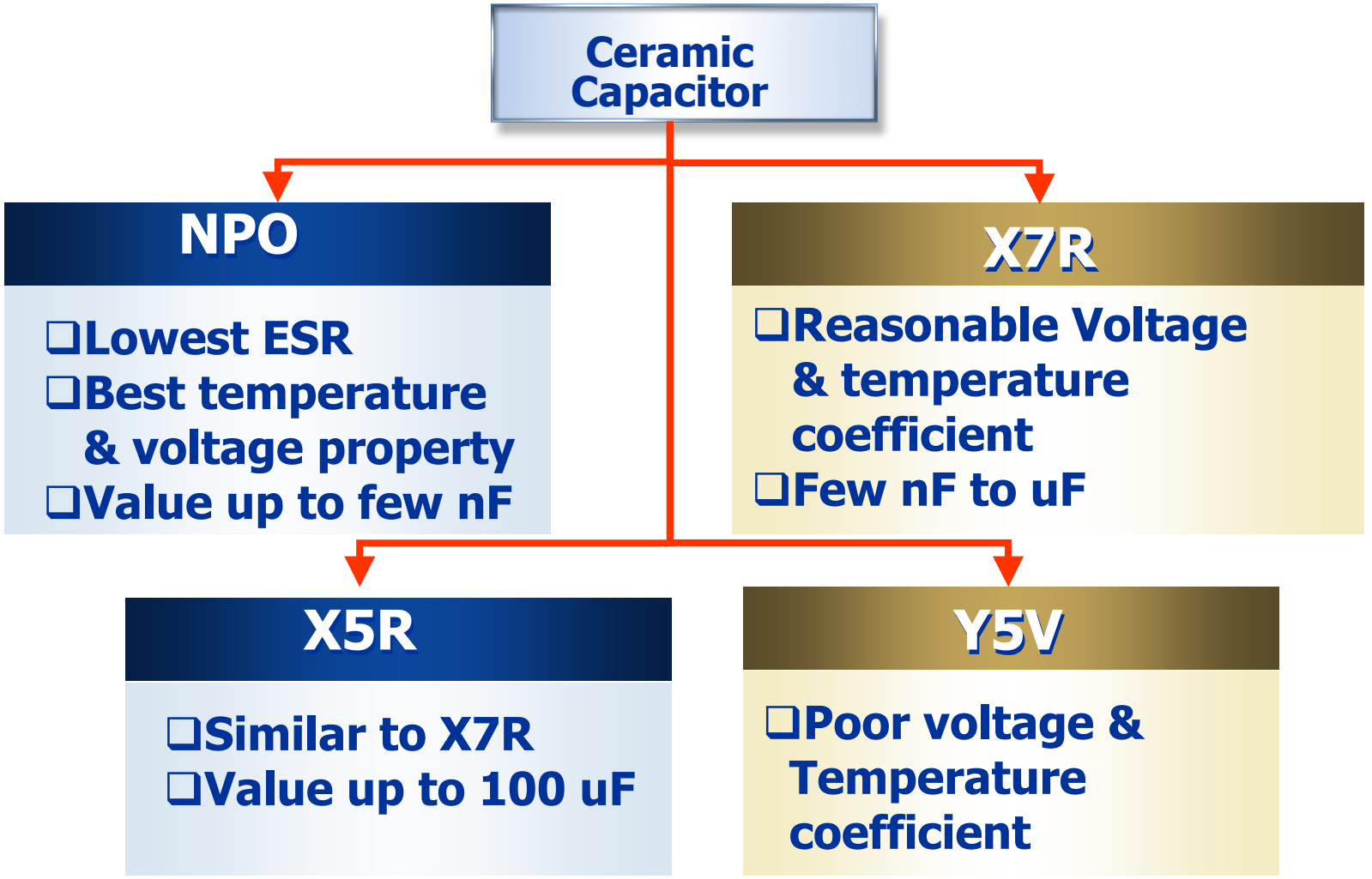
Glass Encapsulated Ceramic

- ❑0.01uF to 0.1 uF
- ❑Chip bypass
- ❑Use with electrolytic to bypass high frequency @ Power bus

Ceramic Chip

- ❑0.01uF to 0.1 uF
- ❑Use at the chip level
- ❑High frequency bypass

Power Supply Filtering



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Cross Talk

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Cross Talk

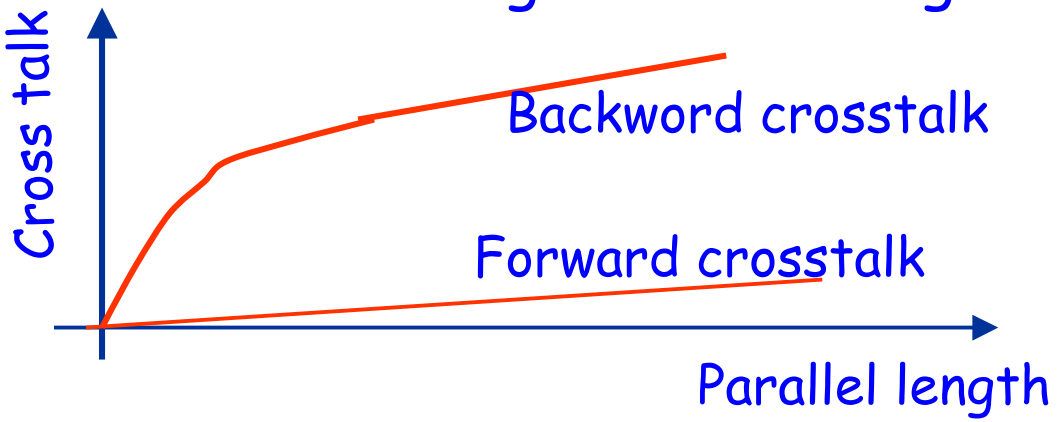
Unwanted signal coupled between traces

Forward (Capacitive) Cross Talk

- Two long parallel traces mutual capacitance between them causing signal cross over

Backward (Inductive) Cross Talk

- Magnetic field (caused by signal traveling) from one trace induced a signal in the neighboring trace



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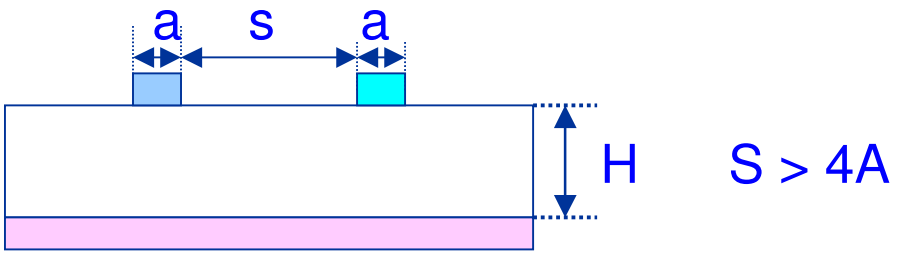
Cross Talk



- Height of trace above the ground plane and dielectric material affect cross talk
- Low dielectric material reduces separation between signal trace and ground

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Ground Bounces

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Ground Bounce

- Fast switching edge causing high transient current in the IC's ground ,together with quick discharge of capacitance load current into the ground develop a transient ground voltage causes ground bounce
- Ensure good ground or use ground plan
- Ensure good decoupling capacitors across device's VCC and Ground and close to the device's lead

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Appendix

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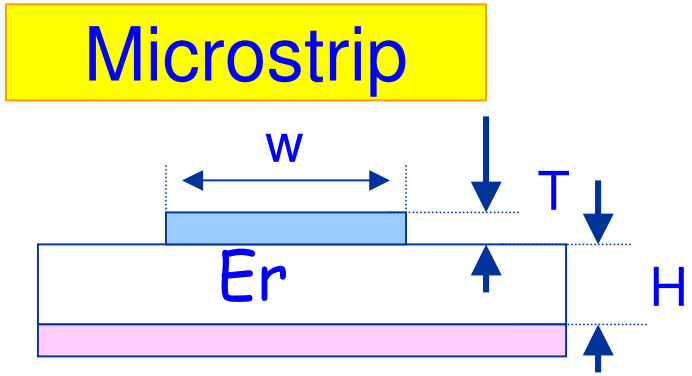
Micro Strip



1 oz copper trace T = 1.4 mil
FR4 material Er = 4.1

Zo = (87 / Sqrt (Er + 1.41)) ln ((5.98 x H) / (0.8W + T))

Co = (0.67 x (Er + 1.41)) / ln ((5.98 x H) / (0.8 x W + T))

Lo = 0.001 x (Co x SUMSQ (Zo)) ????

Tpd = 0.0833 x (1.016 x (SQRT(0.475 x Er + 0.67)))

for W = 8 mil, H = 5 mil, T = 1.4 mil, Er = 4.1 Zo = 49.67 ohm

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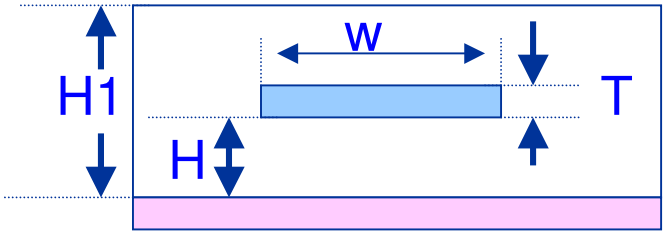
Strip line

Embedded Microstrip



1 oz copper trace T = 1.4 mil
FR4 material Er = 4.1

Er' = Er x (1 – Exp ((-1.55 x H1) / H)))
Zo = (60 / Sqrt (Er')) ln ((5.98 x H) / (0.8 x W + T))
Co = (1.41 x Er') / ln ((5.98 x H) / (0.8 x W + T)))
Lo = 0.001 x (Co x SUMSQ (Zo))) ????
Tpd = 0.0833 x (1.016 x SQRT (Er'))

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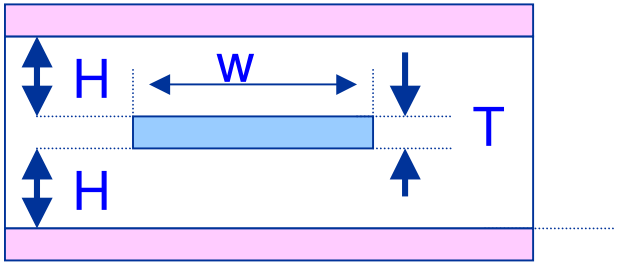
Strip line

Stripline (Symmetic)

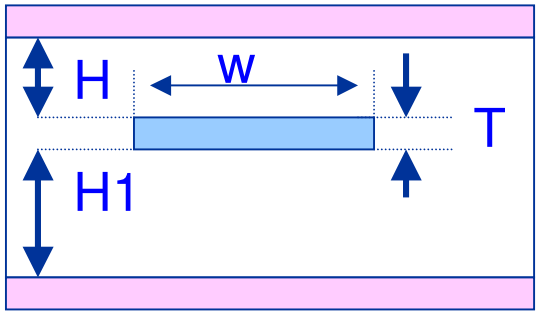


1 oz copper trace T = 1.4 mil
FR4 material Er = 4.1

Zo = (60 / Sqrt (Er)) ln (1.9 x (2 x H + T) / (0.8 x W + T))
Co = (1.41 x Er) / ln ((3.81 x H) / (0.8 x W + T))
Lo = 0.001 x (Co x SUM SQ (Zo))
Tpd = 0.0833 x (1.016 x Sqrt (Er))

Strip line

Stripline Asymetry



1 oz copper trace T = 1.4 mil
FR4 material Er = 4.1

Co = (2.82 * Er) / (ln ((2 * (H-T)) / ((0.268 * W) + (0.335 * T))))

Lo = 0.001 * (Co * SUMSQ (Zo))

Zo = (80/Sqrt(Er)) * ln ((1.9 * (2*H+T)) / (0.8 * W + T)) * (1-(H/(4*H1)))

Tpd = 0.0833 * (1.016*(Sqrt(Er)))

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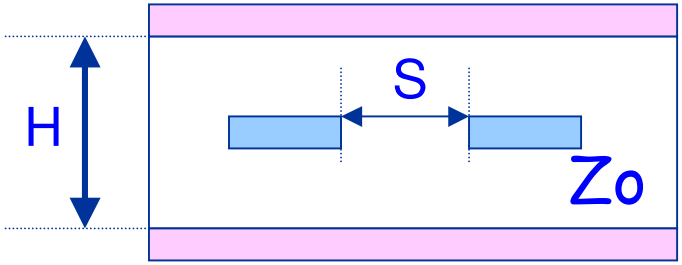
Strip line

Differential Stripline



1 oz copper trace T = 1.4 mil
FR4 material Er = 4.1

Zdiff = 2 x Zo (1-0.347 x Exp (-2.9 x (S / H))))

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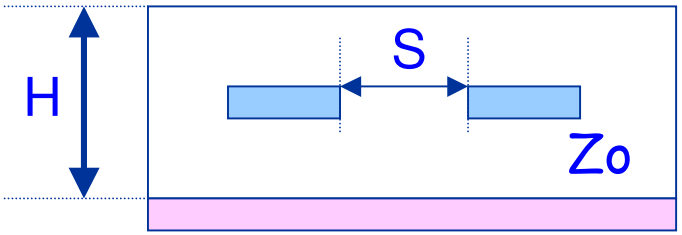
Strip line

Differential Microstrip



1 oz copper trace T = 1.4 mil
FR4 material Er = 4.1

$$Zdiff = 2 \times Zo \left(1-0.48 \times Exp \left(-0.96 \times (S / H) \right) \right)$$

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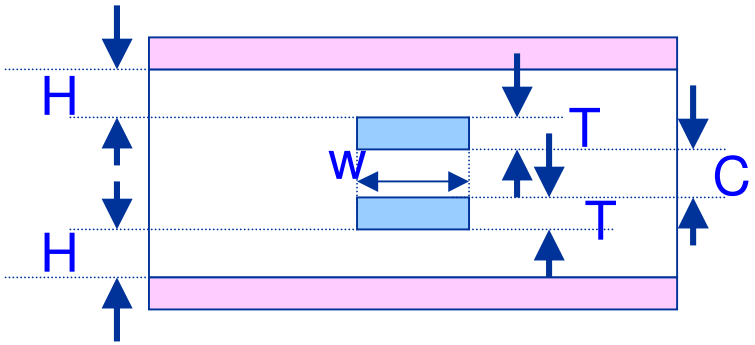
Strip line Impedance

Dual Stripline



1 oz copper trace T = 1.4 mil
FR4 material Er = 4.1

Co = (2.82 x Er) / (ln ((2 x (H-T))/((0.268 x W) + (0.335 x T))))

Lo = 0.001 * (Co * SUMSQ (Zo)) ???

Zo = (80/SQRT(Er)) * ln ((1.9 * (2*H+T))/(0.8*W+T)) *
(1-(H/(4*(H+C+T))))

Tpd = 0.0833 * (1.016 * (SQRT(Er)))

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